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Use of nonstoichiometry to form GaAs tunnel junctions

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A tunnel diode was formed from GaAs containing excess arsenic incorporated by molecular beam epitaxy at reduced substrate temperatures. The incorporation of excess arsenic during growth results in a more efficient incorporation of silicon on donor sites and beryllium on acceptor sites. The better dopant incorporation, along with trap assisted tunneling through deep levels associated with the excess arsenic, results in a tunnel junction with record peak current density of over 1800 A/cm^2, zero-bias specific resistance of under 1×10^{-4} Ω cm, and a room-temperature peak-to-valley current ratio of 28. © *1997 American Institute of Physics.* [S0003-6951(97)04251-4]

High-quality tunnel junctions have a number of applications, including series connections between tandem solar cells, nonalloyed ohmic contacts, digital logic, and high-frequency oscillators. High-quality tunnel junctions are only obtained when very stable, high doping levels can be achieved on both sides of the junction. Improvements in doping efficiency and stability in GaAs have been achieved by growing heavily doped regions at reduced substrate temperatures.[1] Likewise, very low resistance, nonalloyed ohmic contacts to *n*-GaAs have been obtained by utilizing very heavy silicon doping in the depletion region of a tunnel contact in conjunction with low-temperature growth surface stabilization.[2] We have investigated tunnel junctions utilizing both reduced temperature growth and heavy *n*-type doping in the depletion region of the device. We have fabricated tunnel diodes with record peak current densities, zero-bias specific resistances, and peak-to-valley ratios by molecular beam epitaxy (MBE) of the tunnel region at low substrate temperatures.

Forming nonalloyed, low-resistance, ohmic contacts to *p*-GaAs is straight forward because GaAs can be acceptor doped to concentrations that facilitate low-resistance tunneling contacts, and *p*-GaAs is relatively resistant to oxidizing. This is not the case for *n*-GaAs, making nonalloyed contacts more problematic. When the *n*-dopant species (such as silicon on a gallium site) concentration is increased, eventually the dopant begins to substitute on the acceptor sites (such as silicon on an arsenic site) limiting practical net electron concentrations to 5×10^{18} cm^{-3}. This low electron concentration, in conjunction with the fact that *n*-GaAs readily oxidizes, negates the possibility of a simple nonalloyed ohmic contact technology to *n*-GaAs.

There have been demonstrations of nonalloyed ohmic contacts to *n*-GaAs, but the techniques necessary limit the applicability. During MBE of *n*-GaAs, surface states force the Fermi level to be at midgap. In the surface depletion region, silicon can incorporate on gallium (donor) sites to concentrations exceeding 1×10^{20} cm^{-3} because of the negligible concentration of free electrons in the depletion region. As the growth proceeds and the GaAs region with 1×10^{20} cm^{-3} silicon atoms on gallium sites moves through the edge of the depletion region, the large concentration of electrons results in many of the silicon atoms switching to arsenic (acceptor) sites resulting in a much lower net electron concentration ($<5\times10^{18}$ cm^{-3}). Because the donor concentration in the surface depletion region is 1×10^{20} cm^{-3}, the depletion region is narrow enough to facilitate a low-resistance nonalloyed contact. Removing the sample from the MBE system will result in a loss of this narrow depletion region because of the ready oxidation of *n*-GaAs surfaces. By depositing metal *in situ* after MBE of heavily doped *n*-GaAs, Kirchner *et al.*[3] obtained a low-resistance nonalloyed contact since the metal protected the high donor concentration depletion region.

Patkar *et al.*[2] took Kirchner *et al.*'s[3] technique and developed a method for removal from the MBE system prior to the deposition of metal for a nonalloyed ohmic contact. Patkar *et al.*[2] passivated the heavily doped *n*-GaAs with a thin layer of low-temperature grown (LTG) GaAs. This thin LTG-GaAs contains about 1% excess arsenic and prevents surface oxidation because of the short carrier lifetime in this layer.[4,5] Electrons could readily transport through the large concentrations of midgap states in the LTG-GaAs layer[6–8] and then tunnel through the depletion region.

Both Kirchner *et al.*'s[3] and Patkar *et al.*'s[2] techniques for forming ohmic contacts to *n*-GaAs may only be performed on the top surface of the epilayer and do not allow any additional processing to be performed on the top surface prior to metal deposition. GaAs tunnel diodes have been investigated as embedded device interconnects, such as a series connection between solar cells of differing band gaps.[9] Since nonalloyed ohmic contacts can be readily made to *p*-GaAs even after processing of *p*-GaAs surfaces, the combination

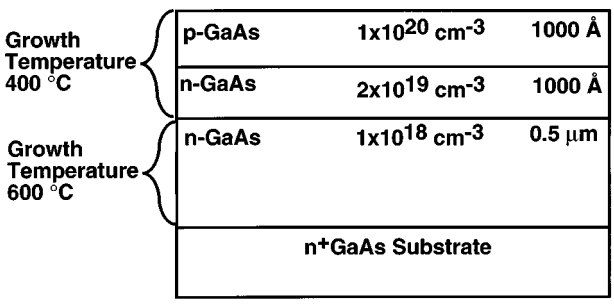

FIG. 1. Cross section of tunnel junction structure.

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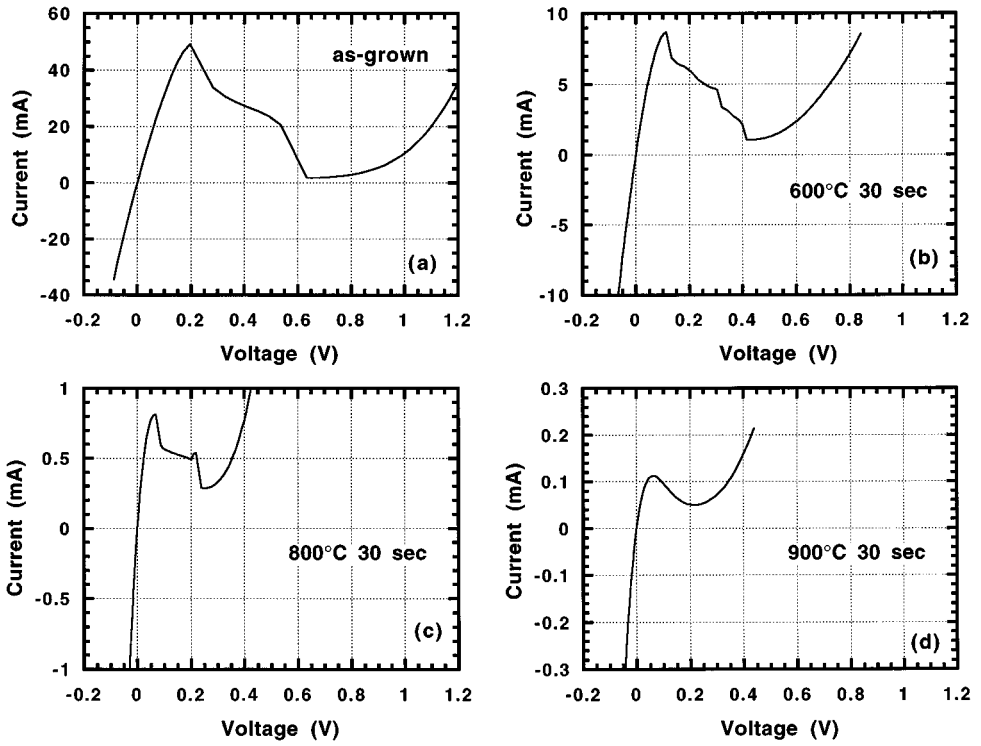

FIG. 2. Current–voltage characteristics of a $45\times60\ \mu m^2$ tunnel junction for different anneal conditions.

of a p-GaAs layer and a tunnel junction could be used to form nonalloyed ohmic contacts to n-GaAs. An application of particular interest to us is the use of tunnel diodes to facilitate low-resistance nonalloyed ohmic contacts to thin-film GaAs p-n junction devices, where a nonalloyed ohmic contact is required to both sides of a thin ($\sim1\ \mu m$) p-n junction.[10]

The tunnel junction is shown in Fig. 1. It was grown in a GEN II MBE system. The tunnel region consisted of 100 nm of p-GaAs ($1\times10^{20}\ cm^{-3}$) and 100 nm of n-GaAs ($2\times10^{19}\ cm^{-3}$). The high silicon concentration was obtained by using a silicon filament as the source.[11] The substrate temperature of 400 °C during growth of the tunnel region insures a higher incorporation of silicon on donor sites (gallium) and beryllium on substitutional acceptor sites (gallium).[1] Note that low-temperature growth incorporates excess arsenic during growth, making dopant incorporation onto gallium sites more likely. In addition, diffusion of dopants is greatly reduced, allowing very abrupt junctions to be produced. The excess arsenic that is incorporated in the tunnel region because of the lower growth temperature[12,13] may also assist in the tunneling process by providing defect assisted tunneling. The back-side contact to the n-GaAs substrate was alloyed indium and the top contact was a nonalloyed Ti/Au tunneling contact to a heavily doped p-GaAs contact layer. The Ti/Au was used as an etch mask for forming individual tunnel diode mesas with wet chemical etching.

Shown in Fig. 2 are the current–voltage (I–V) characteristic for a $45\ \mu m\times60\ \mu m$ tunnel diode for the as-grown structure and after anneals of 600, 800, and 900 °C for 30 s. As the tunnel diode is annealed at progressively higher temperatures, there is a decrease in the peak current density and an increase in the zero-bias specific resistance. The characteristics of the tunnel diode as a function of anneal are compiled in Table I. The as-grown tunnel diode has a peak current density of over $1800\ A/cm^2$ and a zero-bias specific resistance of less than $7.8\times10^{-5}\ \Omega$ cm. This is the highest peak current density and lowest specific resistance ever reported for a GaAs tunnel diode. The best previously reported GaAs tunnel diode had a peak current density of $360\ A/cm^2$ and a zero-bias specific resistance of $1.4\times10^{-4}\ \Omega\ cm$[14] while most other demonstrated tunnel diodes had much lower peak current densities and higher specific resistances.[15–18]

In addition to the record peak current densities and low specific resistance, these tunnel diodes also exhibits a record peak-to-valley current ratio of 28. Such a high peak-to-valley ratio is indicative of a very high quality tunnel junction. The peak current of a tunnel diode may be estimated as in Ref. 19. Even assuming that all incorporated dopants are active, the measured peak current density is an order of magnitude larger than predicted. One possible explanation for the high measured peak current density is trap assisted tunneling where the tunneling current is increased via resonant tunneling through intermediate deep level states inside the depletion region of the junction. In addition, the excess current in the tunnel diode (measured at the valley of the forward current–voltage characteristic) is several orders of magnitude higher than that expected for ideal thermal diode currents. Since the excess current is generally attributed to tunneling through midgap states, this excess current is also an indication of deep levels in the depletion region of the tunnel diode.[17] The excess current is also significantly higher than reported for other high performance GaAs tunnel diodes. The reduction of the excess current with anneal likewise indicates that redistribution of the dopant and defect species during the

TABLE I. Summary of tunnel diode characteristics.

	as-grown @ 400 °C	600 °C 30 s	700 °C 30 s	800 °C 30 s	900 °C 30 s
J peak (A/cm^2)	1824	322	34.3	30.2	4.2
J valley (A/cm^2)	64.7	38.8	11.1	10.8	1.9
Peak-to-valley current ratio	28.2	8.3	3.1	2.8	2.2
V peak (mV)	195	113	71	69	63
V valley (mV)	634	414	260	239	217
$\frac{V \text{ peak}}{J \text{ peak}}$ (Ω cm^2)	1×10^{-4}	3.5×10^{-4}	2.1×10^{-3}	2.2×10^{-3}	1.5×10^{-2}
zero-bias specific resistivity (Ω cm^2)	7.8×10^{-5}	2.1×10^{-4}	9.2×10^{-4}	1×10^{-3}	6.2×10^{-3}

anneal lowers the density of deep levels in the depletion region of the diode.

In summary, we have used low-temperature molecular-beam epitaxy in the production of GaAs tunnel junctions. The excess arsenic during epitaxy results in a more efficient incorporation of silicon on donor sites and beryllium on acceptor sites. Using band-to-band tunneling current calculations, assuming all the silicon dopants are on donor sites and beryllium on substitutional acceptor sites accounts for only 10% of the total peak tunneling current, indicating that the excess arsenic plays a significant role. The better dopant incorporation, along with the arsenic point defects assisting in the tunneling process, results in a tunnel junction with a record peak current density of over 1800 A/cm^2, zero-bias specific resistance of under 1×10^{-4} Ω cm, and a room-temperature peak-to-valley current ratio of 28.

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