# Metal-insulator-semiconductor structure on low-temperature grown GaAs

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The metal-insulator-semiconductor (MIS) capacitors on low-temperature grown (LTG) GaAs were made using the jet-vapor-deposition (JVD) silicon nitride as the gate dielectrics. The unpinned JVD-SiN/LTG-GaAs interface was shown by the capacitance-voltage characterization. The observed Fermi level "pinning" in the unannealed samples was caused by the bulk point defects in LTG GaAs. Annealing reduced the bulk defect density in LTG GaAs and revealed the intrinsically unpinned Fermi level at the interface. The result is consistent with the expected unpinning of LTG GaAs surface, and JVD SiN appears to play a critical role to enable this unpinned interface. JVD SiN showed low leakage current ($\sim$10 nA/cm$^2$ at 2 MV/cm) and high breakdown electric field ($\sim$9.8 MV/cm), promising for MIS device applications. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2404605]

GaAs metal-oxide-semiconductor field-effect transistors have advantages for high-speed and low-power applications;[1] however, their development has been hindered by the gate oxide quality and the Fermi-level pinning. Thermal oxide on GaAs was found to have poor quality,[2] and the oxide/GaAs interface of low-temperature plasma oxidation[3] and anodic oxidation[4] needs further improvement. Therefore, research effort has been focused on deposited dielectrics and metal-insulator-semiconductor (MIS) structures; for example, *in situ* deposited $Ga_2O_3(Gd_2O_3)$ by molecular beam epitaxy (MBE),[5] heteromorphic dielectrics [e.g., $SiO_2$,[6] $Si_3N_4$,[7] and $Al_2O_3$ (Ref. 8)], and wide-band-gap semiconductors used as pseudoinsulators [e.g., AlGaAs (Ref. 9) and ZnSe (Ref. 10)]. In this research, we studied the MIS structure of low-temperature grown (LTG) GaAs with jet-vapor-deposition (JVD) gate dielectrics. LTG GaAs exhibits interesting properties different from those of regular stoichiometric GaAs, including high density of point defects, very short minority carrier lifetime, and inhibited surface oxidation.[11] It has found numerous device applications, including field-effect transistor buffer layers,[12] nonalloyed Ohmic contacts,[13] nonlinear optics,[14] etc. The stable LTG layer can also be applied on regular GaAs for surface preservation. Experiments of Schottky contacts on LTG GaAs indicated unpinned surface Fermi level in LTG GaAs.[15] The MIS structure of LTG GaAs provides more information of the insulator/LTG-GaAs interface properties for potential metal-insulator-semiconductor field-effect transistor devices. JVD technique has been used to deposit high-quality insulators on Si,[16] GaN,[17] and GaP.[18] It utilizes a high-speed jet of light carrier gases to transport depositing species onto the substrate to form insulator films. The separation of depositing species and the short transit time help to minimize the gas-phase nucleation and contribute to the high dielectrics quality.[16]

The GaAs sample was grown by a solid source MBE and the *p*-type substrate was chosen for potential *n*-channel devices. A 400 nm thick regular *p*-type GaAs epilayer doped to $1\times10^{17}$ cm$^{-3}$ with Be was grown on a $p^+$-type GaAs substrate with a 20 nm thick heavily doped ($1\times10^{20}$ cm$^{-3}$) GaAs buffer layer between them. Above the *p* layer, a 3 nm thick surface GaAs epilayer was grown at a lower temperature ($\sim$225 °C) with the Be doping concentration of $1\times10^{20}$ cm$^{-3}$. After growth, the MBE sample was transferred to the JVD system for the deposition of an 8.5 nm thick SiN as the gate insulator, followed by the postdeposition annealing (PDA) in a rapid thermal annealer at 500 °C in $N_2$ for 1 min. Samples without PDA were also made for comparison. Al was deposited on SiN as the gate metal using an e-beam evaporator, and patterned by wet etching to form MIS capacitors. The backside Ohmic contact on GaAs substrate was made with Au–Zn alloy. Figure 1 shows the structure of the Al/SiN/GaAs MIS capacitor.

The capacitance-voltage (*C-V*) characteristics were measured using the HP4284A *LCR* meter. Figure 2 compares the *C-V* characteristics of the Al/SiN/LTG-GaAs MIS capacitors with PDA (square symbols) and without PDA (circle symbols), at the measurement frequency of 10 kHz. The capacitor area is $\sim5.1\times10^{-4}$ cm$^2$. The *C-V* characteristics of the GaAs MIS with PDA demonstrate clear transition from accumulation to depletion/inversion, showing unpinned interface Fermi level of LTG GaAs. The solid line represents

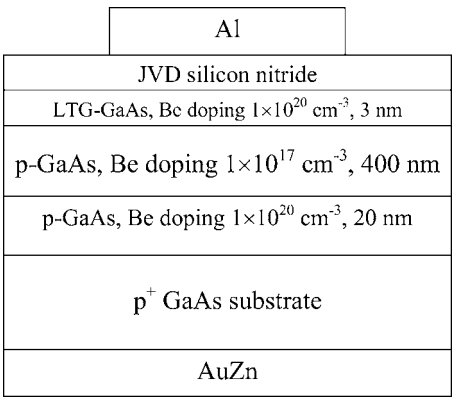


FIG. 1. Structure of the Al/SiN/GaAs MIS capacitor.

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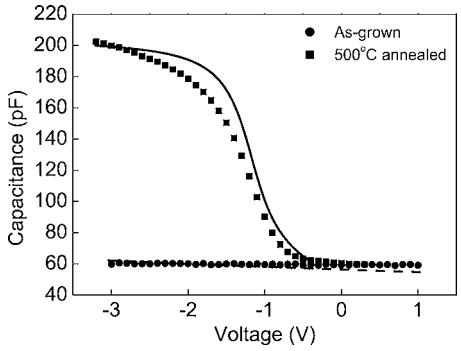


FIG. 2. Measured capacitance-voltage ($C$-$V$) characteristics of as-grown (circle symbols) and annealed (square symbols) GaAs MIS capacitors, with the simulated results (the solid line for ideal MIS and the dashed line for MIS with $D_s=3\times10^{13}$ cm$^{-2}$).

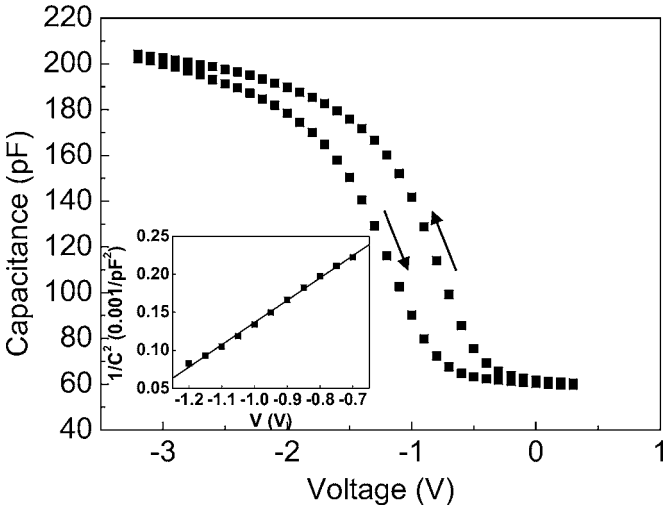


FIG. 3. Measured capacitance-voltage ($C$-$V$) hysteresis of the Al/SiN/GaAs MIS capacitor. The inset shows the $1/C^2\sim V$ fitting in the depletion region.

the simulated $C$-$V$ curve of an ideal GaAs MIS capacitor. The deviation of the experimental results from the ideal $C$-$V$ indicates the existence of oxide charge and interface states. From the flatband voltage shift of ~0.3 V, we estimated the density of fixed charge at the SiN/GaAs interface to be $\sim7.4\times10^{11}$ cm$^{-2}$. This unpinning of interface Fermi level in LTG GaAs is different from regular GaAs as observed in literature, and the difference can be explained by the stable surface and inhibited oxidation in LTG GaAs. Regular GaAs shows severe surface Fermi-level pinning, related to its rapid surface oxidation in air. The oxide/GaAs interfacial reactions generate a mixture of microclusters of different phases whose average work function determines the surface band bending and pins the Fermi level at the oxide/GaAs interface.[19] LTG GaAs contains high density of point defects and has very short minority carrier lifetime (<1 ps), leading to a lower minority carrier concentration near the surface than that in stoichiometric GaAs. Since surface oxidation, primarily via photo-oxidation, requires minority carriers, the surface oxidation rate is much lower in LTG GaAs. Therefore, the surface oxidation in LTG GaAs is inhibited and its surface Fermi level remains unpinned after exposure to air.[20] When the dielectric is deposited at low energy as in JVD, which avoids the heat of condensation, the Fermi level will stay unpinned. Some recent results also suggested that the JVD process played a critical role in enabling this unpinned interface.[21]

On the other hand, the sample without annealing (circle symbols in Fig. 2) shows almost no capacitance modulation by voltage and the surface appears "pinned" in depletion. The difference between the samples with and without PDA can be explained by the bulk defects in as-grown LTG GaAs. As-grown LTG GaAs contains excess arsenic (1%–2%) that results in high density of point defects ($\sim1\times10^{20}$ cm$^{-3}$), mainly arsenic antisites.[22] A thin surface layer with such a high density of point defects contributes to a high density of interface states in the MIS structure. Using the thickness of 3 nm of the LTG layer and the bulk defect density of $1\times10^{20}$ cm$^{-3}$, we can estimate an effective interface state density $D_s$ to be $\sim3\times10^{13}$ cm$^{-2}$. The dashed line in Fig. 2 is the simulated $C$-$V$ of a GaAs MIS capacitor with the interface state density of $3\times10^{13}$ cm$^{-2}$, showing the same "pinning" effect observed in the measurement. Annealing can dramatically reduce the bulk defect density in LTG GaAs and minimize their effects as interface states on the MIS capacitors; therefore, the unpinned interface Fermi level was observed from the $C$-$V$ characteristics of the annealed devices. It is expected that the effective interface state density, which is related to the bulk defects in LTG GaAs, can be optimized by the design of the LTG layer and the annealing conditions. The detailed mechanism of defect reduction by annealing is under investigation, and one explanation is the outdiffusion of excess arsenic through the insulator during annealing.

The interface state density in the annealed MIS capacitors can be estimated from the $C$-$V$ hysteresis measurement, as shown in Fig. 3. The gate voltage was swept from negative to positive, and back to negative. When the sweeping rate of the gate voltage is fast enough, the different charging status of the interface states in the two voltage sweep directions cause a hysteresis gap. From the hysteresis voltage gap of 0.5 V in Fig. 3, we can estimate the interface state density to be $\sim1.2\times10^{12}$ cm$^{-2}$. The interface states come from both the LTG GaAs surface states and its bulk defects reduced by annealing; therefore, the density of surface states of LTG GaAs is expected to be on the order of $10^{12}$ cm$^{-2}$ or lower. The $C$-$V$ characteristics of a MIS capacitor in the depletion region can be used to calculate the doping concentration of the semiconductor substrate. As shown in the inset of Fig. 3, the $1/C^2$-$V$ dependence in the depletion region follows a straight line whose slope is determined by the epilayer doping concentration. The doping concentration of the GaAs epilayer calculated from the $1/C^2$-$V$ fitting is $1.4\times10^{17}$ cm$^{-3}$, very close to the value of $1.7\times10^{17}$ cm$^{-3}$ measured by electrochemical $C$-$V$. The simple $C$-$V$ hysteresis measurement provides first-order estimation of the interface properties. More sophisticated measurements, including multifrequency $C$-$V$ and quasistatic $C$-$V$, are under investigation to further characterize the interface quantitatively.

The unpinned interface Fermi level can also be verified by the dependence of $C$-$V$ characteristics on different work functions of gate metals. MIS capacitors with Ni gate were made to compare with the capacitors with Al gate. The difference on the flatband voltages of the Ni-gate and the Al-gate capacitors was measured to be ~0.5 eV, while the work function difference between Ni and Al is ~0.9 eV. Although not proportional to the gate metal work functions due to the existence of interface states, the flatband voltages show the trend of modulation by the gate metals and confirm that the

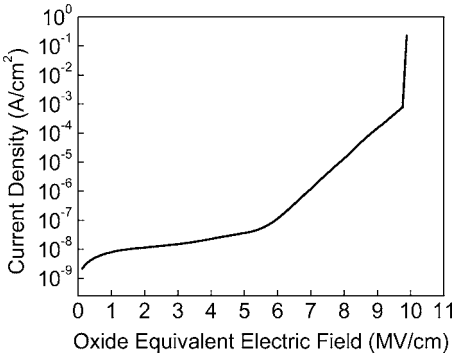


FIG. 4. Measured current-voltage ($I$-$V$) characteristics of the Al/SiN/GaAs MIS capacitor.

surface Fermi level of LTG GaAs is unpinned.

The current-voltage ($I$-$V$) characteristics measured using the HP4156A parameter analyzer are shown in Fig. 4. It demonstrates similar features observed on the JVD SiN grown on Si, GaN, and GaP,[16–18] indicating high reliability of JVD thin film on various semiconductor substrates. The JVD SiN on LTG GaAs shows low leakage current of $\sim 10\ \mathrm{nA/cm^2}$ at the oxide equivalent electric field of 2 MV/cm, which is desirable for low-power applications. The breakdown electric field of JVD SiN is measured to be $\sim 9.8$ MV/cm, higher than that of other deposited dielectrics previously reported.[4,7,8]

In summary, we demonstrated an unpinned MIS structure on LTG GaAs using JVD SiN as the gate dielectrics. The pinning in the unannealed sample was caused by the bulk point defects in the as-grown LTG GaAs layer. Annealing dramatically reduced its bulk defect density and revealed the intrinsically unpinned surface Fermi level in LTG GaAs. The unpinned surface Fermi level of LTG GaAs is consistent with the stable surface of LTG GaAs. The JVD technique is found to be critical in enabling the unpinned interface. The unpinned LTG surface layer may be utilized to preserve the surface of regular GaAs from oxidation and Fermi level pinning, opening a wide range of potential device applications.

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