InGaP/GaAs/InGaP double-heterojunction bipolar transistors grown by solid-source molecular-beam epitaxy with a valved phosphorus cracker

T. P. Chin, J. C. P. Chang, and J. M. Woodall

School of Electrical and Computer Engineering and the MRSEC for Technology-Enabling Heterostructure Materials, Purdue University, West Lafayette, Indiana 47907-1285

W. L. Chen^{a)} and G. I. Haddad

Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan 48109

(Received 18 September 1995; accepted 17 November 1995)

The growth and device characterization of an InGaP/GaAs double-heterojunction bipolar transistor is reported, the device is grown in a solid source molecular beam epitaxy system equipped with a valved phosphorus cracker. Various designs of base–collector (B-C) junction are used to eliminate the current blocking effect caused by the conduction band discontinuity. The results show that a chirped superlattice with a delta-doping layer at the B-C junction has the best dc characteristics. Both dc and microwave results of these devices are comparable to those obtained with other advanced growth techniques. © 1996 American Vacuum Society.

I. INTRODUCTION

Solid-source molecular-beam epitaxy (MBE) using valved crackers has been demonstrated to be a viable technique for the growth of device-quality phosphorus-containing compounds.¹⁻⁴ The growth of high-performance InGaP/GaAs and InGaAs/InP single-heterojunction bipolar transistor (SHBT)⁵⁻⁷ as well as optical devices⁸ by a valved phosphorus cracker have been reported. In this article, we present the growth and device performance of InGaP/GaAs/InGaP double-heterojunction bipolar transistors (DHBTs) grown by a valved phosphorus cracker.

InGaP/GaAs/InGaP DHBTs have been investigated for high power and high speed applications, such as high efficiency microwave amplifiers. Using InGaP as the collector material is essential to achieve such goals because it has a high breakdown voltage. However, the conduction band discontinuity at the base-collector (B-C) junction, though smaller than that in the AlGaAs/GaAs system, can still have a significant electron-blocking effect and results in poor I-Vcharacteristics at low V_{ce}. Various junction designs have been used to reduce this effect. The first design investigated in this work is to insert a small-band-gap spacer layer and a heavily *n*-type wide-band-gap layer between the base and the collector to reduce the effective conduction barrier. The second design is to use a composition-graded junction between the narrow-band-gap base and the wide-band-gap collector. This method has been commonly used in AlGaAs/GaAs HBTs. However, it is very difficult to achieve a true compositional grading between InGaP and GaAs because they do not share the same anion. Therefore, a chirped superlattice (CSL) structure has to be used to simulate a compositional grading layer. Finally, since a quasielectric field exists within the grading region due to the conduction band discontinuity, further improvements are made in the third design. In this structure, an *n*-type delta doping layer (*inm*) is inserted under the CSL. This n^+ layer and the p^+ base generate an opposite electric field, which compensates the quasielectric field at the junction. We found that the doping dipole does decrease the current blocking effect while decreasing the breakdown voltage somewhat. The application of the CSL and doping dipole in InGaP/GaAs DHBT was recently demonstrated by Liu *et al.* with gas-source MBE.⁹ Cowles *et al.* also demonstrated an InAlAs/InGaAs DHBT with linearly graded B-Cjunction and a pulse doping layer by solid-source MBE.¹⁰

II. EXPERIMENTAL DETAILS

The growth was performed in a modified Varian GEN-II chemical-beam epitaxy (CBE) system, which has been described elsewhere.⁵ A valved cracker was used as the phosphorus source, while standard effusion cells were used for As, Be, and group-III metals. A Si filament was used as the *n*-type doping source. P₄ molecules were thermally cracked into P₂ at 900 °C before being injected into the growth chamber. The typical phosphorus beam equivalent pressure was $1-2 \times 10^{-5}$ Torr. Reflection high-energy electron diffraction (RHEED) oscillations were used to calibrate growth rates, compositions, and surface V/III ratio. The typical growth temperature for InGaP was around 520 °C. The full-width at half-maximum (FWHM) of the x-ray rocking curve of a $1-\mu$ m-thick InGaP film is 24 arcsec. The photoluminescence linewidth of an undoped InGaP layer is 12 meV at 10 K. Transmission electron diffraction pattern of InGaP layers indicates that this material has a short-range ordered structure,⁵ which has a normal bandgap as opposed to the smaller band gap of long-range ordered InGaP. This is consistent with the PL measurements which show normal band-gap energy.

Figure 1 shows the general device structure for this study. This DHBT was grown on a GaAs(100) substrate. The thickness of the GaAs base was 65 nm. A 5-nm-thick undoped GaAs layer was grown to prevent Be from diffusing into the InGaP emitter. The only difference between the three devices

^{a)}Current address: Central Research Lab, Texas Instruments, Dallas, TX 75265.



FIG. 1. Structures of devices A, B, and C.

is at the B-C junction. Device A utilizes a spacer layer as described in the previous section. Device B has a CSL layer between the base and the collector. Within the CSL, the thicknesses of the GaAs and InGaP in monolayers (MLs) are 1,1,2,2,...,9,9 and 9,9,8,8,...,1,1, respectively. A 1 s interruption was included between each layer. The total thickness of the CSL is 51 nm. Device C has the same CSL layer and a 1 nm heavily doped *n*-type layer underneath.

Transmission electron microscopy (TEM) micrographs of device C at (010) direction were taken. Figure 2(a) shows the dark-field TEM image over a large area of the device. Each layer, including the CSL, can be seen clearly. Figure 2(b) shows the lattice image of the CSL layer. InGaP and GaAs appear in different ([002] vs [022]) lattice fringes. These are due to the large difference in the amplitude of [002] and [022] type diffracted waves between the ternary and binary crystals for a given specimen thickness. The selective-area [001]-zone axis diffraction pattern of the CSL layer is shown in Fig. 2(c), where extra spots along [200] direction is observed. This is due to the well-controlled 10 ML periodicity within the CSL layer.

The InGaP DHBTs were processed using a self-aligned process. Selective etchant HCl:H₃PO₄ was used for removing InGaP over the GaAs while H₃PO₄:H₂O₂:H₂O was used to etch GaAs over InGaP. Furthermore, the chirped superlattice region between the base and collector was etched nonselectively with saturated bromine water solution. Pd/Ge/Ti/Au and Pt/Ti/Pt/Au were used for emitter (collector) and base ohmic contacts, resulting in contact resistivity of around 8×10^{-7} (6×10⁻⁷) and 3×10⁻⁶ Ω cm², respectively. After the deposition of the ohmic contacts, SiO₂ was deposited by plasma-enhanced chemical vapor deposition. Then via holes were opened by reactive-ion etching. Finally, Ti/Al/Ti/Au was used for interconnect metal for dc and microwave probing. Specially designed masks were used for optimized microwave performance. Figure 3 shows the scanning electron micrograph of a transistor with emitter and base aligned in the (011) direction. This orientation reduces the etching undercut, so smaller B-C capacitance can be achieved. The separation between the emitter mesa and the base metal is less than 0.15 μ m.

One of the advantages of InGaP/GaAs HBTs over





(b)



FIG. 2. (a) Dark-field TEM image of device C. (b) The lattice image of the CSL layer. InGaP and GaAs appear in different ([002] vs [022]) lattice fringes. (c) Selective-area [001]-zone axis diffraction pattern of the CSL layer, where extra spots along the [200] direction due to the well-controlled 10 ML periodicity within the CSL layer is observed.



FIG. 3. Scanning electron microscopy (SEM) pictures of a 32 μ m² device. The base and emitter are aligned along (010) and (001) planes.

AlGaAs/GaAs HBTs is that good selective etchants between InGaP and GaAs are available. However, the intermixing of phosphide and arsenide at the InGaP/GaAs interface may still cause problems during the wet etching process. If the GaAs surface is exposed to a phosphorus beam first at the collector/subcollector or emitter/base interface, we would observe a nonuniform etching. This is attributed to the formation of a GaP-like interface due to its relatively high bond strength. Our experiments show that this intermixing problem can be eliminated if 1 ML of group-III metal is deposited before the phosphorus shutter is opened while growing phosphides on arsenides. The same growth sequence is also used



FIG. 4. dc characteristics of devices A, B, and C.



FIG. 5. Gummel plot of a large-area ($40 \times 40 \ \mu m^2$) device C.

in InP/InGaAs HBT structures, and similar effects are achieved.

III. RESULTS AND DISCUSSIONS

Figure 4 shows the dc characteristics of all three devices with emitter area of $40 \times 40 \ \mu m^2$. Device A shows a large saturation voltage (V_{sat}), or knee voltage, (>10 V) and a small Early voltage with breakdown voltages $V_{ceo} \approx 20$ V and $V_{\rm cbo} \approx 30$ V. The carrier blocking effect at the B-C junction is clearly observed. The saturation voltage of device B is greatly reduced to ≈ 0.8 V. The dc current gain is about 50 and the breakdown voltages are $V_{ceo} \approx 26$ V and $V_{cbo} \approx 32$ V. The improvement of the breakdown voltages comes from the use of an undoped collector layer without any heavily doped region. The CSL layer effectively reduces the electron barrier at the B-C junction. Negative differential resistance is also observed in the I-V curves due to the electron tunneling through the mini subbands of the CSL layer. This has been reported in InP/InGaAs HBT with a CSL layer at the B-Ciunction.11

Device C shows the best turn-on characteristics. The I-V characteristics look similar to those of a SHBT with better breakdown voltages. The saturation voltage drops to 0.4 V while the offset voltage is less than 0.2 V. The output conductance of the transistor is very small, resulting in a large Early voltage. The maximum dc current gain is also increased to 60 due to less electron blocking at the B-C junction. The ideality factors for collector and base current are 1.00 and 1.50, respectively (Fig. 5). The only drawback of this design is that the breakdown voltages decrease to $V_{ceo} \approx 20$ V and $V_{cbo} \approx 28$ V because of the delta-doping layer near the B-C junction. It is possible to fine-tune the device to achieve required performance by changing the delta-doping concentration.

Smaller-sized device C (emitter area=32 μ m²) was fabricated for microwave measurements. On-wafer *S*-parameter measurements were performed from 0.5 to 26.5 GHz. From the measured *S* parameters, the short circuit current gain ($|h_{21}|^2$) and power gain (*U*) were calculated at different frequency and bias conditions. Then 20 dB/decade extrapolation is used to estimate the current gain cutoff frequency (f_t) and maximum oscillation frequency (f_{max}). The highest f_{max} and f_t are around 72 and 32 GHz, respectively. The bias



FIG. 6. Cutoff frequency (f_t) and maximum oscillation frequency (f_{max}) of a 32 μ m² device at different bias conditions.

dependent f_t and f_{max} are plotted in Fig. 6. The f_t decreases with V_{ce} because of the increasing collector depletion width and increasing collector transit times. On the other hand, f_{max} initially increases with V_{ce} due to the reduced C_{bc} . As V_{ce} further increases, the increasing collector transit time becomes dominant, thus f_{max} starts to drop as shown in Fig. 6(b).

IV. CONCLUSION

We demonstrated that the valved-phosphorus cracker is comparable to other phosphorus sources used in gas-source MBE or CBE for growing complicated structures requiring monolayer thickness control. The first InGaP/GaAs DHBT grown by solid-source MBE was realized in this work. Various kinds of B-C junction layer including a chirped superlattice and delta doping were used for optimized dc and microwave performance. V_{sat} as low as 0.4 V and high breakdown voltages were achieved, along with $f_t=32$ GHz and $f_{\text{max}}=72$ GHz.

ACKNOWLEDGMENTS

The work at Purdue University was supported by a Materials Research Science and Engineering Center from the National Science Foundation No. DMR-9400415. The work at the University of Michigan was supported by ARO under URI program Grant No. DAAL03-92-G-0190 and ARPA under Contract No. DAAH-04-93-G-0242.

- ¹G. W. Wicks, M. W. Koch, J. A. Varriano, F. G. Johnson, C. R. Wie, H. M. Kim, and P. Colombo, Appl. Phys. Lett. **59**, 342 (1991).
- ²D. J. Mowbray, O. P. Kowalski, M. S. Skolnick, M. C. DeLong, M. Hopkinson, J. P. R. David, and A. G. Cullis, J. Appl. Phys. **75**, 2029 (1994).
- ³D. J. Mowbray, O. P. Kowalski, M. Hopkinson, and M. S. Skolnick, Appl. Phys. Lett. **65**, 213 (1994).
- ⁴J. N. Baillargeon, A. Y. Cho, F. A. Thiel, R. J. Fischer, P. J. Pearah, and K. Y. Cheng, Appl. Phys. Lett. **65**, 207 (1994).
- ⁵T. P. Chin, J. C. P. Chang, J. M. Woodall, W. L. Chen, G. I. Haddad, C. Parks, and A. K. Ramdas, J. Vac. Sci. Technol. B **13**, 750 (1995).
- ⁶T. P. Chin, J. M. Woodall, W. L. Chen, and G. I. Haddad, presented in 1995 Electronic Material Conference (unpublished).
- ⁷W. E. Hoke *et al.*, J. Vac. Sci. Technol. B **13**, 733 (1995).
- ⁸J. A. Varriano et al., Proc. SPIE 1788, 21 (1992).
- ⁹T. Liu, C. Nguyen, and H-C. Sun, presented at the 1995 Electronic Materials Conference, Charlottesville, VA, June 1995 (unpublished), p. A8, paper E3.
- ¹⁰J. Cowles, L. Tran, T. Block, D. Streit, and A. Oki, presented at the 53th Annual Device Research Conference, Charlottesville, VA, June 1995 (unpublished), p. 84, IVA-4.
- ¹¹C. Nguyen, H-C. Sun, and T. Liu, in Ref. 10, p. 82, IVA-3.