A 2DEG/LOW-TEMPERATURE-GROWN GaAs DUAL CHANNEL HETEROSTRUCTURE TRANSISTOR

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Dual channel transistor structures utilizing real-space-transfer (RST) offer the potential for fast switching and negative differential resistance. We have built a two channel heterostructure field effect transistor (FET) incorporating a modulation doped 2-dimensional electron gas (2DEG) and a thin channel of low-temperature-grown GaAs containing As precipitates. The low mobility characteristic of low-temperature-grown GaAs provides a large mobility ratio, which is a prerequisite for a high speed, mobility modulation transistor utilizing RST.

A series of dual channel FET structures with different channel lengths has been fabricated and characterized by capacitance-gate voltage, transconductance, and current-voltage measurement. These measurements, performed over a 77-300K temperature range, confirm the presence of two distinct channels separated by a 6nm AlAs layer. Carrier concentration versus depth was determined using a layer-by-layer depletion approximation. Mobility as a function of depth was then calculated using transconductance. A 2DEG/low-temperature-grown GaAs channel mobility ratio of 41 was measured at 77K.

Introduction

One technology with great high-speed potential as well as good 3-dimensional chip utilization is the two channel transistor. Extremely fast switching is possible due to the small vertical distances attainable between channels. The transport of carriers perpendicular to their usual channel is known as real space transfer (RST) [1-5]. Using MBE or CVD techniques, channel separation distances of hundreds of Angstroms are readily achievable. This translates to inter-channel flight times in the hundreds of femtoseconds. Further, negative differential resistances have been measured in two channel transistors due to the increase in inter-channel movement as carriers are heated by transverse electric fields [6,7].

One class of these RST devices, the mobility- or velocity-modulation transistor (VMT), requires the close proximity of two channels whose mobilities or carrier drift velocities differ significantly [2]. Such a transistor could be switched quickly by moving carriers vertically between the "on" state, when they occupy the fast channel, and the "off" state, when they are in the slow channel. The greater the difference in electron velocities within the two channels, the greater the corresponding change in current when the state is switched. However, a prominent characteristic of this device is that its switching time is not limited by transconductance, as it is in field effect transistors (FETs).

The main focus of this work is to develop a material system for the VMT. Specifically, a 41 fold mobility ratio has been achieved in a GaAs/$Al_xGa_{1-x}As$ system between a 2-dimensional electron gas (2DEG) in an undoped GaAs layer and a reduced mobility channel containing arsenic precipitates [8].

A series of two channel FETs have been fabricated, as described below. Capacitance, I-V and transconductance measurements were performed at temperatures between 77K and 300K in order to characterize the structures. Electron density and mobility were calculated as functions of position. The buried Schottky model [9] successfully predicts the effects of localized As precipitates on carrier density throughout the entire heterostructure.

To form As precipitates, a portion of the film is grown by MBE at a reduced temperature, generally 200 - 250°C; 1-2% excess As is incorporated into that part of the film. When annealed, the As atoms form clusters. The size and, consequently, the surface area of these clusters depend on the anneal temperature and time. The As precipitates are suspended in the regular GaAs matrix and act as buried Schottky surfaces, complete with associated surface states.

One effect of the precipitates is a reduction in carrier concentration that depends on the total precipitate surface area. Electron mobility is also reduced. Low-temperature-grown (LT) GaAs containing As precipitates is particularly well suited for use as the low speed channel because it can support a high density of electrons while incorporating a large number of closely spaced precipitates. Most of the samples in these experiments were annealed by RTA such that their precipitate densities were about $9x10^{15}/cm^3$ [9]. Additionally, measurements were performed on devices that had not been annealed following removal from the MBE system. In these samples, the *in situ* anneal caused the formation of smaller precipitates with a density of about $1.7x10^{17}/cm^3$ [9].

The fact that mobility and carrier concentration can be varied with anneal conditions as well as with dopants gives LT GaAs versatility useful in the design of RST transistors. Additionally, LT GaAs has the same electron affinity as GaAs. This fact can clearly facilitate efficient bi-directional transfer of electrons between channels.

Fabrication and Test

The two channel heterostructure is shown in Figure 1. It consists of a normal 2DEG and a low-temperature-grown GaAs channel separated by a 60 Å

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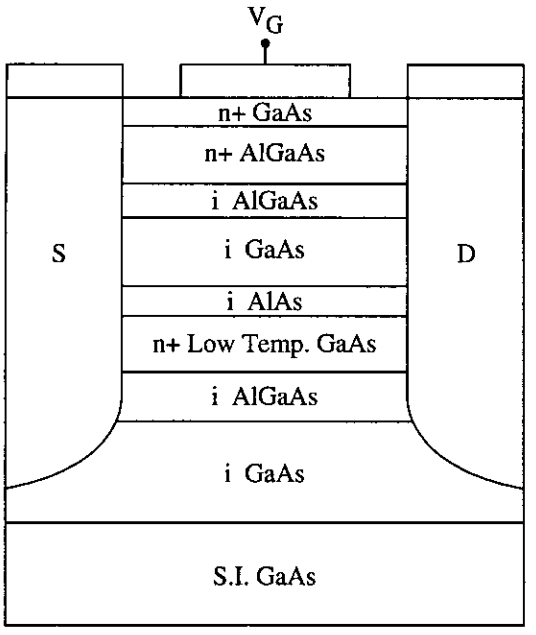

Figure 1. Cross-section of the two channel FET.

AlAs barrier. The heterostructure was grown in a Varian GEN II MBE system on a 2-inch diameter semi-insulating GaAs substrate. The bottom two layers were grown at 600°C, the normal growth temperature. These layers were 1 um of undoped GaAs and 200 Å of undoped $Al_{.4}Ga_{.6}As$. Next, the low mobility channel was grown at 250°C - 200Å GaAs, doped with $1x10^{18}/cm^3$ Si. Growth was then interrupted while the temperature was increased. The top epilayers were 60Å of undoped AlAs, 200 Å of undoped GaAs, a 50 Å buffer layer of undoped $Al_{0.3}Ga_{0.7}As$, a 600 Å donor layer of $Al_{0.3}Ga_{0.7}As$ doped $1x10^{18}/cm^3$ Si, and finally a 50 Å cap of GaAs doped $1x10^{18}/cm^3$ Si. The arsenic enriched LT GaAs was, of course, exposed to the 600°C final growth temperature, causing precipitates to form during epitaxial growth [9]. The AlAs was designed to physically separate the channels and to keep excess arsenic from migrating into the undoped GaAs.

Later, the wafer was cleaved. One piece was annealed at 800°C to cause the excess arsenic to aggregate into larger clusters with a diameter on the order of the thickness of the low mobility channel. Another piece of the wafer was fabricated into devices without further high temperature treatment beyond the 600°C *in situ* anneal. The samples were mounted onto a silicon wafer using indium. Source and drain contacts of gold-germanium eutectic were evaporated then sintered at 425°C for four minutes. Conductive mesas were defined by wet chemical etch. The FETs' top gates, which were gold over titanium, were deposited next. The gates were optically aligned and ranged in size from 2 x 37 um to 20 x 70 um^2. Large Hall bars were fabricated as well. The chips were then diced, mounted into DIPs and wire bonded for test.

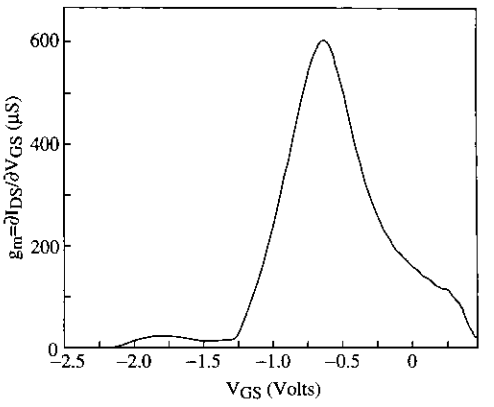

Figure 2. Double peaked transconductance versus gate voltage, measured at 77K for the 800°C annealed sample.

A variety of measurements were made on these dual channel structures, both the 800°C annealed FETs and the as-grown FETs. Source, drain and gate currents were measured as functions of V_{ds} and Vgs using an HP4145B Semiconductor Parameter Analyzer. For these tests, the temperature was varied from 300K down to 77K. The devices were cooled by mounting the DIPs onto the cold finger of a recirculating helium cryostat. The cryostat had a window that allowed the cooled transistors to be exposed to light. Transconductance versus gate voltage was also measured at these temperatures. Capacitances were measured as a function of gate voltage over the frequency range of 10^4 to 10^7 Hz using an HP4275A LCR meter. Capacitance was measured at 300K and at 77K by placing the DIPs in a liquid nitrogen bath. Additionally, Hall measurements were performed in a cryostat using a 0.4 T electromagnet.

Results and Analysis

It is clear from the double peaked transconductance curves that two channels are present. Figure 2 presents the double peaked graph for the 800°C annealed FET measured at 77K, with the deeper channel having lower conductivity than the 2DEG. The 300K transconductance plot of the 800°C annealed FET has a similar double peak, as seen in Figure 3. The 600°C annealed FET (not shown) has only the single peak, as does a simple FET. Later, it will be shown that the smaller, more numerous precipitates in the 600°C sample deplete both the LT and 2DEG channels. Transconductances displayed in Figures 2 and 3 were measured at low source-drain voltages to facilitate mobility calculations. The double peaks are also very evident when the FETs are biased into saturation.

Electron concentration as a function of depth, n(x), was computed from C-V measurements. The relation $C=\varepsilon A/x$ was used determine depth. Electron concentration was determined using a relation derived from the expression in [10],

$$n(x) = \frac{C^3}{A^3 q \varepsilon}\left(\frac{dC}{dV}\right)^{-1} , \qquad (1)$$

namely,

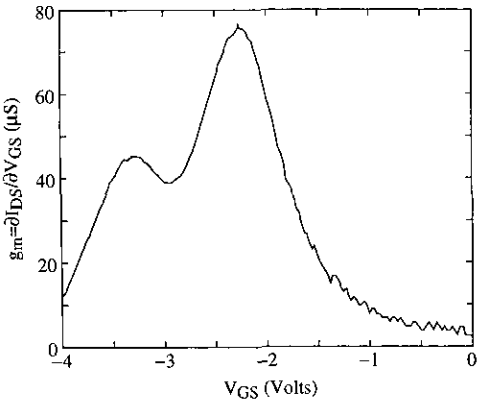

Figure 3. Double peaked transconductance versus gate voltage measured at 300K for the 800°C annealed sample.

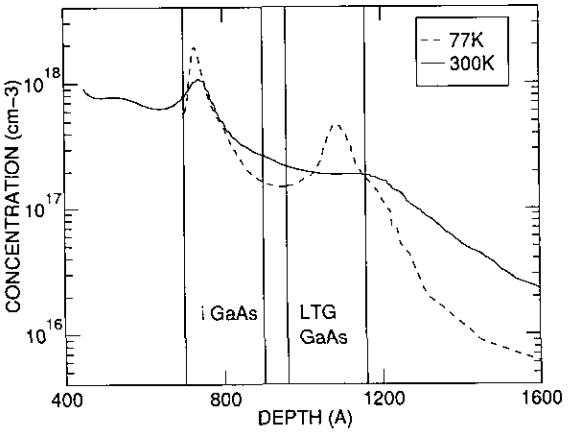

Figure 4. Measured electron concentration in the 800°C annealed sample.

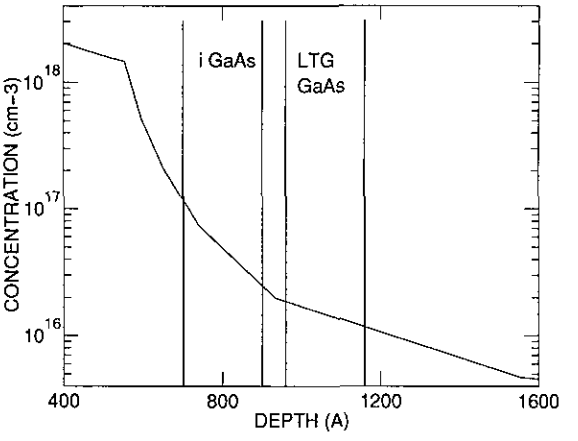

Figure 5. Measured electron concentration in the 600°C annealed sample.

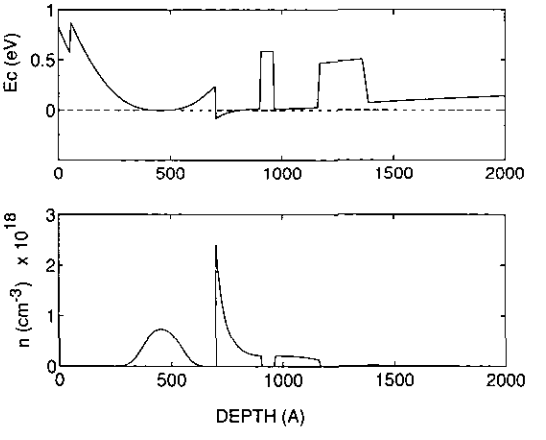

Figure 6. Theoretical prediction of E_C and n(x) for the 800°C annealed sample.

$$n(x) = \frac{-C}{qA}\left(\frac{dx}{dV}\right)^{-1} . \qquad (2)$$

The results of these calculations for the 800°C are shown in Figure 4. The above calculations are reliable unless the semiconductor has large swings in electron concentration over distances shorter than a few Debye lengths,

$$L_D = \left(\frac{kT\varepsilon}{q^2 n}\right)^{\frac{1}{2}} , \qquad (3)$$

which causes n(x) to appear to be somewhat smeared rather than abrupt [10]. For a region with $n(x) = 2x10^{17}$, L_D = 97 Å at 300K and L_D = 49 Å at 77K. Consequently, the 77K graph shows more detail than the higher temperature curve, including the reduced electron concentration in the AlAs barrier region and the two peaks in the channels. The 300K sample has a parasitic MESFET region in the $Al_{0.3}Ga_{0.7}As$ which is frozen out at 77K.

Figure 5 shows the measured n(x) for the 600°C sample. The large number of small arsenic precipitates in the LT layer have entirely depleted both the LT layer and the 2DEG, leaving only the parasitic MESFET. Changing the anneal temperature has a profound effect on the distribution of electrons in the 200 Å LT region as well as the rest of the device.

Both sets of n(x) measurements support the modeling of arsenic precipitates as buried Schottky barriers suspended in a GaAs matrix [9]. A Schottky barrier height of 0.7 eV and TEM measurements of precipitate size and distribution as functions of anneal temperature found in [9] were used to determine the average effective charge in the LT layer. For example, the average precipitate diameter in the 800°C material was 15 nm. Poisson's equation for a spherical Schottky barrier of that size yields about 80 electrons on each precipitate. Multiplying by the precipitate density of $9.3x10^{15}/cm^3$ yields $7.4x10^{17}/cm^3$. Coupled with $1x10^{18}/cm^3$ donors, that leaves $2.6x10^{17}/cm^3$ free

electrons in the LT GaAs, in excellent agreement with the measured data shown in Figure 4. A 1-dimensional semiconductor-Poisson solver [11] was used for analysis. The Schottky barriers and ionized donors were modeled together as an effective compensation dopant density in the LT layer. The resulting conduction band diagrams and carrier distributions are shown in Figures 6 and 7 for the 800°C and 600°C anneals, respectively. The theoretical free electron sheet concentrations in the two channels agree well with the measured data. The concentration of electrons in the doped $Al_{0.3}Ga_{0.7}As$ was higher than predicted in the 600°C sample.

Because the depletion caused by the LT layer was not greater than predicted, it can be concluded that the AlAs was an effective barrier to excess As migration. Had an appreciable amount of As escaped into the AlAs or i-GaAs layers, the total depleting capacity of the precipitates would have increased. Precipitates would be smaller, more numerous and some would have been closer to the 2DEG and unscreened by ionized donors.

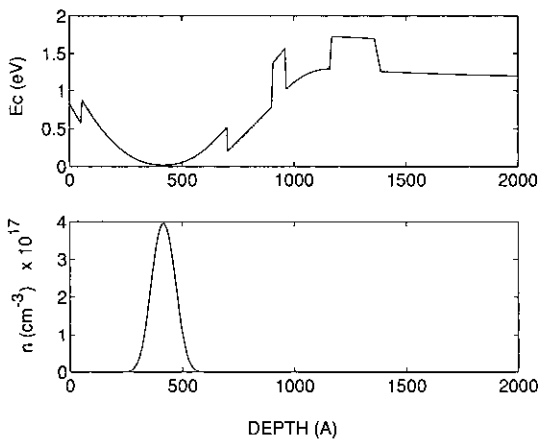

Figure 7. Theoretical prediction of E_C and n(x) for the 600°C annealed sample.

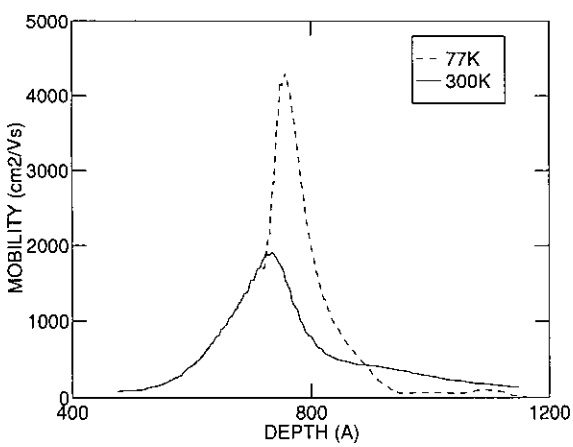

Figure 8. Measured mobility in the 800°C annealed sample.

Figure 8 presents mobility data for the 800°C annealed sample. Mobility was determined by a capacitance-conductance method. Transconductance, g_m, was measured at low source-drain bias. The electric field across the channels, E_y, was assumed to be uniform. The calculation follows, using w=width.

$$g_m = \frac{\partial I_{ds}}{\partial V_g} = \frac{\partial}{\partial V_g}\left[w \int E_y \, q \, n(x) \, \mu(x) \, dx \right] \quad . \tag{4}$$

Rearranging (4),

$$\mu(x) = \frac{g_m}{qwn(x)E_y}\left(\frac{dx}{dVg}\right)^{-1} \quad . \tag{5}$$

In the 800°C sample, the mobilities of the channels were drastically different from each other, as expected, with a ratio of 41:1 at 77K and about 5:1 at 300K, even though all mobilities were smaller than anticipated. The 2DEG mobilities were quite low, especially at 77K, indicating the presence of traps. It is unlikely that the As precipitates in the LT layer were the cause of the reduced mobility in the 2DEG since the LT layer was separated from the 2DEG by about 180 Å. This distance is sufficient separation between a high mobility 2DEG and Coulomb scatters of $1x10^{18}/cm^3$ density [12]. It is possible that there was increased scattering due to traps may have formed in the i-GaAs because of growth interruption, reduced temperature or thermal transients that occurred after the LT GaAs was grown. The mobility of the 800°C annealed LT GaAs was lower than reported elsewhere [9] by a factor of 4 at 300K. This may be explained to some extent by the slightly smaller carrier density in our LT layer, which would reduce screening. Additionally, our LT GaAs was only 200 Å thick, so surface states caused by growth interruption would have a larger effect than on a thicker sample.

Discussion

Figure 9 diagrams a planned two channel VMT. The RST transistor switches state by moving carriers back and forth between fast and slow channels as outlined in [2], using transverse fields generated at the top and bottom gates. A similar RST transistor was analyzed by Monte Carlo methods [13] and found to be capable of 2 ps switching, which is faster than the source-drain transit time. The 2 ps figure exceeds the inter-channel time-of-flight by a factor of ten, with the bulk of the switching time expended in redistributing the transferred electrons inside the target channel. The current difference between on and off states in that simulation was calculated to be 40% using a modulation doped channel and a compensation doped channel. The 2DEG-LT GaAs material system outlined in this paper provides a large room temperature mobility ratio between channels and should be capable of producing greater current modulation in a VMT as well as extremely fast switching.

Negative differential resistance was not observed in the I_{ds} versus V_{ds} plots. Low mobility inhibited hot-electron induced RST [1,3,4,14] over the large AlAs barrier. However, with appropriate modification to the layer structure, specifically the replacement of the AlAs with a reduced potential barrier, and the addition of a back gate, hot electron RST should be attainable in a comparable material system.

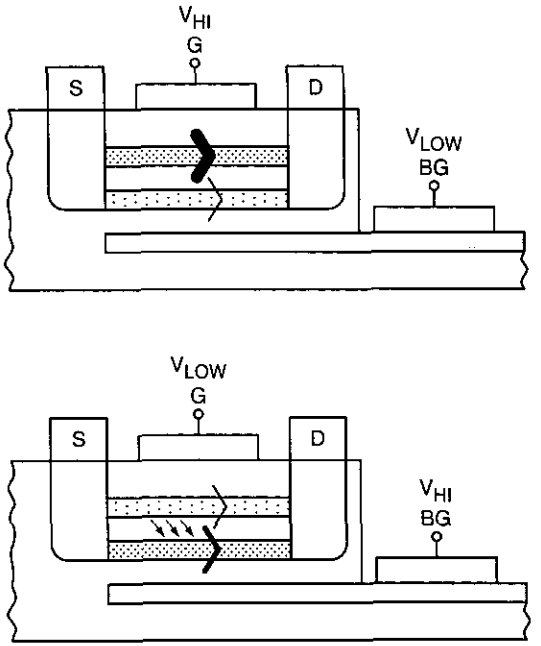

Figure 9. Dual channel, dual gated velocity modulation transistor. Top: Transistor biased to the "on" position. Bottom: Transistor is switched to "off" by swapping the gate voltages.

Another advantage of a 2DEG-LT GaAs system in a double gated VMT is the fact that the mobility difference between channels is large while the electron affinities are the same. There is no conduction band discontinuity inherent between channels. A heterostructure compatible with Figure 9 would necessarily be designed without an AlAs layer. This fact will keep the gate voltages required for switching from being too large.

In this paper, the high potential barrier of the AlAs acted to separate the 2DEG from the LT channel and their mobilities could be measured without use of a back gate. Such a barrier is not required in the planned double gated structure. 2DEG mobilities must be improved to approach the levels found in single channel devices [12] in order to produce the best results in a VMT.

Conclusion

We have built a two channel FET consisting of a GaAs/$Al_xGa_{1-x}As$ system containing a 2DEG and a reduced mobility channel containing arsenic precipitates. The static effects of As precipitates on carrier density in the channels have been successfully predicted by a simple buried Schottky model. The As precipitates have been confined to the low mobility channel by an AlAs barrier. We have measured large mobility ratios between channels, which indicates that a similar two channel system would perform well in a VMT. The LT GaAs/2DEG is made more versatile by the ability to manipulate carrier densities and mobilities by varying anneal temperatures.

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