Transport Properties of a Superconductor-Semiconductor Ohmic Contact

A. Davidson, M.J. Brady, D.J. Frank, J. M. Woodall,

and A. Kleinsasser

IBM Research, PO Box 218, Yorktown Heights, NY 10598

Abstract

We report electrical measurements of a sandwich structure consisting of a niobium electrode in contact with a thin lightly doped n type InGaAs layer. The bottom of the sandwich is a degenerate layer of n-type InGaAs used to collect the current. The semiconductor layers are grown by molecular beam epitaxy (MBE). These three layers are the essence of the proposed superconducting-base, semiconductor-isolated transistor (SUBSIT), lacking only the emitter tunnel junction. It could also form the basis for a superconducting FET type device. We have observed a resistance rise, beginning just below the transition temperature of the niobium, and continuing to at least 2 K. Nonlinear IV curves are also measured, and may be interpreted in some instances as space charge limited current flow.

Introduction

Contacts between superconductors and semiconductors have been proposed for use in 3 terminal amplifying and switching devices for at least the last ten years. Silver and his group[1,2] at Aerospace proposed an FET-like device in which the charge induced on the semiconductor surface by a gate potential would modulate the proximity effect on the semiconductor surface. T.D. Clark[3] proposed a similar device at around the same time. More recently, Frank[4] and co-workers proposed a bipolar-like mechanism that would use the semiconductor to isolate the superconductive base from the collector. This device has been named SUBSIT (for Superconducting-Base Semiconductor-Isolated Transistor).

Experimentally, Silver could demonstrate a reduction in resistance in his devices on InAs, but never demonstrated a supercurrent. Such supercurrents have now been observed in silicon and in both p type and n type InAs by Nishino[5], Takayangi[6] , Kawakami[7] and Kleinsasser[8]. Experimental work on the bipolar mechanism has been reported by Kobayashi[9], and by Tamura[11]. In no device, of either bipolar or field effect design, has useful gain been achieved.

We have been studying the properties of a niobium contact to a ternary semiconductor, n type $In_{85}Ga_{15}As$. Such a contact could eventually form the base-collector structure of a bipolar SUBSIT, or a source or drain contact in an FET type device. Our experiments show that the proximity effect is not necessarily as simple in a semiconductor contact as it is in contacts to normal metal. Our work shows that the theory of the superconductive proximity effects needs to be extended to cover the situation when the "normal metal" is actually a semiconductor. In particular, we observe a resistance increase below the critical temperature of the superconductor, rather than a decrease as the usual proximity effect theory and some other measurements would lead one to expect.

Manuscript received September 30, 1986

Structure

Layers

Our samples are similar to those measured by others in that the contact of interest is between a deposited layer of niobium and a semiconductor surface. Our samples differ from the FET work, however, in that we pass current through and measure voltage across a thin semiconductor layer that is in contact to a thick degenerate layer underneath. That is, our samples have a sandwich structure, with the semiconductor layer of interest between deposited niobium above and degenerate semiconductor below. As shown in the cross section in Fig. 1, we have used 100 nm thick niobium, 200 nm thick semiconductor and 1000 nm thick degenerate layer.

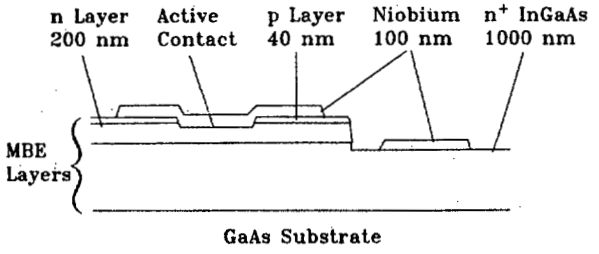

Fig. 1. Schematic cross section of our samples.

Our structure is also different from earlier SUBSIT types in that we have carefully chosen the semiconductor to have its Fermi level pinned in the conduction band at the metal interface. The InGaAs semiconductor layers were grown by molecular beam epitaxy (MBE) on GaAs substrates. This was done to assure the highest quality single crystal samples with a buried degenerate layer. The degenerate layer was doped to 10^{18} n type, and the active layer was 10^{16}. A third p type layer, 40 nm thick, was grown on top of the n type active layer. This p type layer was calculated to be depleted, and so was intended as a surface insulation and passivation layer.

The energy band structure that we estimate for this system is shown in Fig. 2. This diagram is calculated for the active area, and therefore does not show a passivation layer. The conduction band in the InGaAs was assumed pinned at -50 millivolts at both the Nb interface and at the junction with the n+ layer. The Nb and n type layers are shown to scale, but only the first 100 nm of the n+ layer are shown. The dotted conduction band assumed an undoped semiconductor, while the solid line corresponds to a doping of 10^{16}, which is the nominal composition of the material in our experiments. For a good SUBSIT we would like the conduction band to cross the Fermi level. The Superconductor is represented here in the "semiconductor model" in which the electron-like and hole-like bands are shown separately above and below the Fermi level.

Patterns

We have made two types of sample patterns: a cross configuration, (not shown); and a row pattern, Fig. 3. The cross pattern involved etching down to the degenerate layer everywhere except in

0018-9464/87/0300-0727$01.00

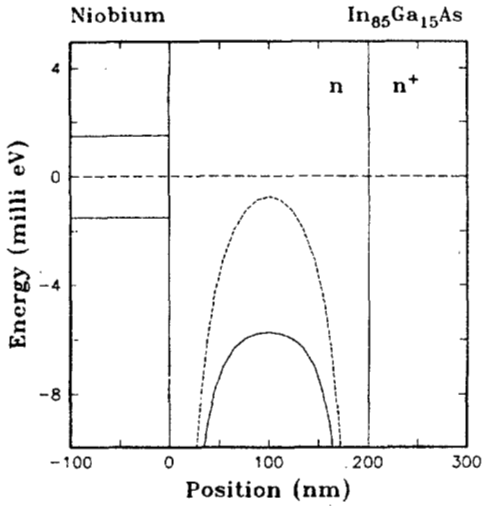

Fig. 2. Energy diagram for a section through the window in the p type layer. The horizontal dotted line is the Fermi level. The two curves in the n type region are for the conduction band under different doping conditions. The dotted curve is for negligible doping, while the solid curve assumes $n=10^{16}$, corresponding to our present devices. Ideally we would like the conduction band to rise a fraction of a millivolt above the Fermi level.

a cross shaped region. The four arms of the cross were left with all the semiconductor layers intact, but a square region 250 microns on a side in the cross's center was etched through the top player down to the n region. Nb was deposited also in a cross pattern inside the semiconductor cross. The active region was in the center, where the Nb was in contact to the n layer.

The cross pattern was useful in obtaining hall effect data to verify the semiconductor doping levels, but presented problems for other electrical measurements because the degenerate level was continuous--there was no way to isolate the current flow and so obtain accurate 4 probe measurements. To improve this isolation the second pattern was chosen, which allowed parallel rows of contacts, 4 for the Nb , 6 for the degenerate layer, and 2 others for testing the quality of the surface passivation. These rows were separated by trenches etched all the way through the degenerate layer. The trenches were used to force the flow of current in the degenerate layer to be confined between specific pads, and therefore to improve the 4 probe measurements. The active device area was 250x25 microns in this row pattern.

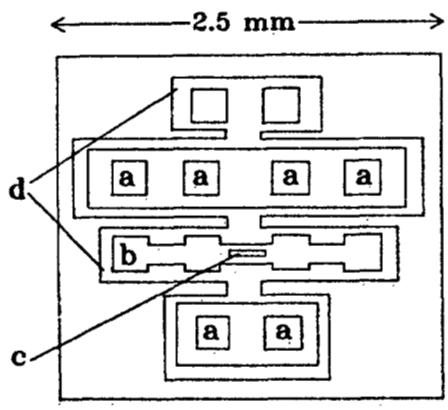

Fig. 3. Schematic of the row pattern which improved the isolation of the measurements by etching trenches down to the semi-insulating substrate. (a) represents contacts to the n+ layer. (b) is a niobium strip with room for four pads. (c) is the p window, and (d) shows the regions where the p layer was left intact. The trench structure is seen surrounding the 12 pads.

Processing

The MBE grown layers of $In_{85}Ga_{15}As$ were made on a semi-insulating GaAs substrate. In spite of the large lattice mismatch between InGaAs and GaAs of 5.88 %, the quality of the epilayers is satisfactory for these experiments because band pinning effects at dislocations do not form Schottky barriers. There is a considerable effect on mobility, however, as discussed later. Silicon was the n type dopant, and magnesium was the dopant for p type. The wafers were 1 cm square, and were diced into 2.5 mm chiplets for further processing. We made one junction and all its associated connections (12, altogether) per chiplet. Exposure of the photoresist was by microscope projection, since contact techniques are not practical with such small samples.

The area to become the window in the p layer was patterned with photoresist and etched in phosphoric, peroxide, and water, exposing the n layer in a small area for eventual contact to Nb. Then regions for contact to the n+ layer were delineated photolithographically, and etched.

The next step was the cleaning of the InGaAs surface prior to the Nb deposition, by one of four methods described below. Nb was then deposited in one layer, contacting the n InGaAs, and the n+ InGaAs. We have successfully patterned the niobium by lift-off, and by dry etching in $CF_4 + O_2$ The Nb was deposited by electron-beam evaporation, with a base pressure of about $4x10^{-8}$ Torr and an oxygen partial pressure of less than $2x10^{-10}$ Torr. On oxidized silicon wafers our niobium had a transition temperature of 9.4 K. On the GaInAs, transitions temperatures were typically 8.9 K. The process was completed by patterning resist to define the isolation trenches, and chemical etching down to the semi-insulating substrate.

Measurements

Mounting

Connecting leads to these samples is a problem. Because of the thin layers of semiconductor at the surface, compression or ultrasonic wire bonding might cause shorts. Therefore we have used a flip-chip technique[10]. Basically, a printed circuit is fabricated on a sapphire wafer so that there are small pads (100 microns square) aligned with each of the niobium pads on the InGaAs chiplet. The patterned sapphire wafer is coated with solder flux and dipped in eutectic Pb-Sn solder at about 250 C. As the sapphire is withdrawn from the solder, mounds of solder adhere to the pads, and less to the narrow (50 micron) lines. The sapphire wafer can be aligned with the SUBSIT chip by viewing the chip directly through the transparent sapphire. The chip is pressed against the solder bumps on the sapphire wafer using a brass bridge, torque screw and copper pressure block[12]. This method has a high yield of good contacts, and withstands several thermal cycles to helium temperature without readjustment.

The samples were secured to a temperature controlled stage in a vacuum can immersed in a liquid helium dewar that could be pumped down to 2 K. Temperature was monitored with a Ge resistance thermometer, and the substrate could be heated electrically to about 20 K. Current, voltage, differential resistance, and temperature could each be measured independently. Data were averaged and recorded digitally using a micro computer and high resolution analog-to-digital converter.

Surface Preparation

Our data depend strongly on the surface preparation of the n-type semiconductor prior to deposition of the Nb. At various times we have tried 4 surface preparations: pure argon sputter cleaning; oxygen plasma cleaning; etching in dilute HF just before loading in the vacuum system; and oxygen plasma cleaning followed by a dip in dilute HF.

Our oxygen plasma cleaning was done in an LFE Corporation barrel reactor, with a 50 sccm flow rate, at 200 Watts. (At these settings our reactor could strip baked 1350 photoresist at an initial rate of 90 Angstroms/minute.) The argon sputter cleaning was done in situ at 20 mTorr of argon, for three minutes at -120 volts self bias. The chemical etching was done with H_2O:HF of 10:1 for 30 seconds,

followed by a rinse in 18 megohm deionized water, and nitrogen blow dry. Getting the samples from the water into the vacuum chamber and pumped down to 10^{-5} Torr took less than 5 minutes.

The differential resistance as a function of bias voltage under the four different cleaning conditions is shown in Fig. 4. We see a range of behavior starting with what is clearly an S-I-N junction at high resistance, down to some fairly low contact resistance levels with the HF treatment.

Let us consider the high resistance curve, which was the result of treatment in a pure oxygen plasma. The reason to use an oxygen plasma is to burn off any organic residue that might be left from patterning the photoresist. However, it may be expected that an oxygen plasma will form a thin oxide on the surface of the semiconductor. The high resistance curve from Fig. 4 shows that a surface barrier to electrons exists after treatment with an oxygen plasma. Evidence is discussed below that indicates this barrier is due to a surface oxide, and not a Schottky barrier.

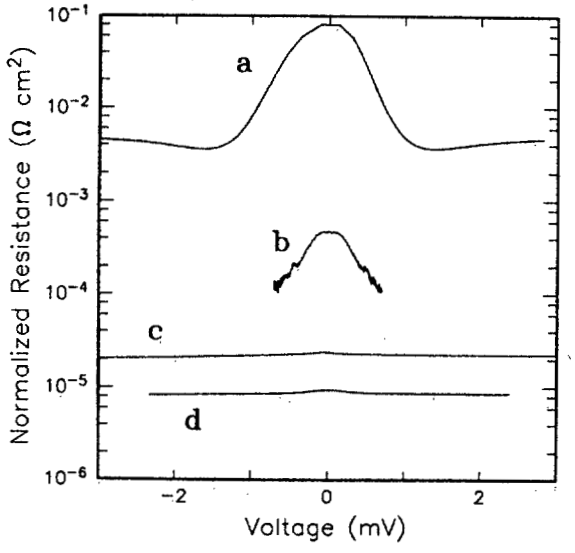

Fig. 4. Differential resistance normalized to the p window area for four devices that received four different surface treatments prior to Nb deposition. Curve (a) is for pure oxygen plasma treatment. (b) corresponds to plasma etching in pure argon. (c) was treated in dilute HF. (d) received first an oxygen plasma treatment and then etched in dilute HF. The cross pattern was used for (a) and (b), while the row pattern was used for (c) and (d).

S-I-N Junction

Fig. 5 is a replot of the data for the high resistance curve of Fig. 4, but now plotted as conductance versus voltage. The superconducting energy gap is clearly seen at the voltage corresponding to the peak in conductance. In fact this curve suggests that the oxygen plasma created a rather high quality SIN tunnel junction, where the N is the surface conducting layer on the semiconductor. The voltage drop is primarily across the tunnel barrier, which dominates the resistance of the contact. We believe that this surface tunnel barrier is related to the oxide and not to a Schottky barrier because the conductance increases as the oxide is removed.

This increase in conductance is shown by the other three curves in Fig. 4. The curve for the sample treated with an an argon sputter clean step shows much lower resistance, and the samples treated with dilute HF show the lowest resistance. The one with dilute HF after an oxygen plasma clean has the lowest resistance, and is in fact getting into the range of the lowest contact resistance with conventional alloyed NiAuGe contacts to GaAs. Furthermore, the samples treated with HF show no changes in conductance that could be associated with the superconducting energy gap. This is reasonable evidence that the conductance of the samples with the cleanest interfaces are not limited by tunneling.

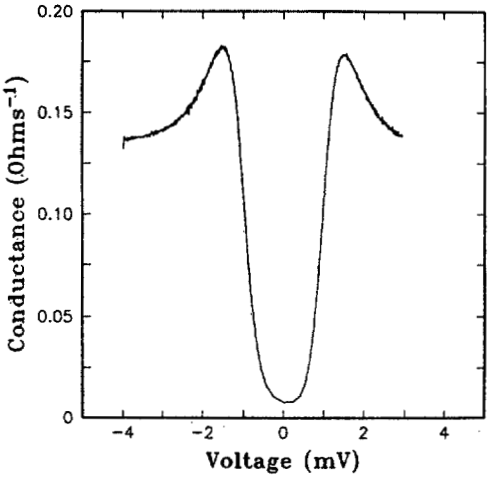

Fig. 5. Replot of oxygen plasma treated sample (curve (a) in Fig. 4.) showing S-I-N tunnel junction characteristic.

Resistance Rise

The next thing to notice about our data is that as the surface barrier disappears, we never see the resistance at zero bias decrease, as would be expected from the usual proximity effect theory. Instead we see the resistance rise. This is shown in Fig. 6 even more clearly, which plots the differential resistance of the highest conductivity sample as a function of temperature. The effect is even larger in the sample treated with the pure argon sputter cleaning step, but data at higher voltages were not taken for that device. (It is possible that it would show gap structure, and so indicate an SIN tunnel junction.) This resistance rise has been a consistent observation in all our samples.

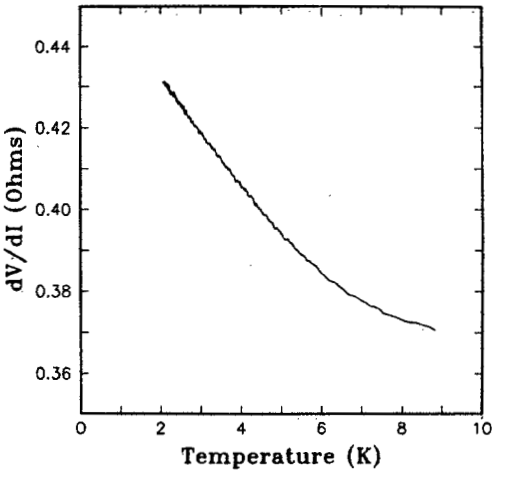

Fig. 6. Temperature dependence of zero bias resistance for our lowest resistance sample, which had an oxygen plasma treatment followed by etching in dilute HF (curve (d) in Fig. 4.).

Space Charge Limited Current Flow

As the current density in the semiconductor increases, the net charge carried by the current begins to affect the field acting on charges at the interface with the niobium. This is embodied in Poisson's and Maxwell's equations, and in the simple case where the current dominates the charge, and where transport is by drift, leads to a relation between voltage, current, and mobility[13]:

$$\mu = \frac{8L^3 J_F}{9\varepsilon_r \varepsilon_0 V_F^2} \qquad (1)$$

Here J_f is the current density in the semiconductor, V_F is the voltage difference across the semiconductor, L is the thickness of the semiconductor, and ϵ_r, ϵ_0, and μ are the usual relative dielectric constant, dielectric constant of free space, and electron mobility in InGaAs. This result means that for a constant mobility, the voltage will tend to saturate, increasing as the square root of the current.

The sample from Fig. 4 that was treated with a pure argon sputter cleaning step, seems to show such behavior. Fig. 7 is based on I-V curve measurements of this contact at various temperatures, and shows V^2/I plotted against current. A tendency toward constant V^2/I is clearly evident, especially at lower temperatures, as the current is increased. Putting in the ratio of V^2/I from the curve at 2.3 K into Eq. 1 along with appropriate dimensions yields a mobility of 4200 cm^2 V sec. This number seems somewhat low for such a material at low temperature, but considering the likely dislocation density of the epi-layer it is reasonable. Kleinsasser has measured a similar mobility for pure MBE grown InAs at 77 K[8].

As mentioned earlier, we did not take data for this sample at higher voltage because of heating effects. Therefore it is premature to claim with certainty that these curves in Fig. 7 truly reflect space-charge limited current flow, and not just a coincidental fit.

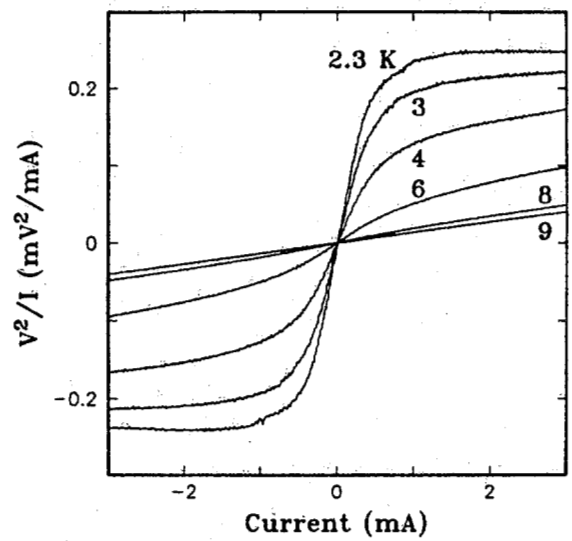

Fig. 7. V^2/I versus current for the sample corresponding to curve (b) in Fig. 5. That the low temperature curves flatten out is evidence for space charge limited current flow in the n type layer.

The Proximity Effect

The rise in resistance that we measure, even in samples with very clean interfaces is a puzzle. The rise is always observed to begin at the critical temperature of the superconductor, and we have not observed any sudden temperature dependent phenomena associated only with the semiconductor. The rise start smoothly at Tc; there is not a sudden jump to a new steady value when the niobium goes superconducting. This strongly suggests that the thermally excited quasiparticles above the superconductor's energy gap are having an large influence on transport through the interface.

This kind of influence, of course, is exactly what would be expected for an S-I-N tunnel junction, and we cannot be absolutely certain about the cleanliness of the contact. However, a tunnel barrier would be expected to reveal itself with structure measured on the IV curve at the voltage corresponding to the magnitude of the gap in the superconductor.

One possibility is that there is indeed a proximity effect induced on the semiconductor surface, but the closeness of the conduction band to the Fermi level in the center of the n type layer limits the range of Cooper pairs. This would leave the quasiparticles above the induced gap free to cross over the maximum in the conduction band, and conduct current to the degenerate collector layer. Hence, as the temperature is lowered, the quasiparticle density drops and the resistance rises. This could be checked experimentally by combining the FET type and SUBSIT type structure. Two superconducting contacts on the surface could detect a proximity effect there, while the buried collector could look for a resistance rise for conduction over the top of the conduction band. This would be a very interesting experiment.

It is worth noting here that although the low density of states in the semiconductor guarantees a low density of pairs due to the proximity effect, this does not necessarily mean a small value of the superconducting gap energy. Crudely speaking, the pair density, n_s is related to the gap Δ by the density of states N:

$$n_s = \Delta N \qquad (2)$$

In a normal metal, N is usually about as large as the normal density of states in the superconductor, so that a small n_s implies a small gap. In the semiconductor, however, since N is also small, the gap may in fact be large--up to the full value in the niobium.

Conclusions

Existing surface measurements and theory suggest that our measurements of a superconductor-semiconductor contact ought to show evidence of the proximity effect, whose signature would be a decrease in resistance below the transition temperature of the superconductor. Instead we see a rise in resistance below T_c even for our cleanest interfaces. Moreover, the differential conductance shows no hint of structure due to the superconducting energy gap, consistent with a very clean interface. Our observations are encouraging for the SUBSIT because they show that quasiparticles above the superconductor's energy gap have a large influence on conductance through the interface.

Acknowledgements

G.D. Pettit grew the MBE films. Several niobium depositions were done by R. Sandstrom. Useful discussions with S. Raider, C. Guarnieri, and B. Bumble are acknowledged.

References

1. A.H. Silver, A.B. Chase, M. McColl, and M.F. Millea, in Future Trends in Superconductive Electronics, B.S. Deaver, C.M. Falco, J.H Harris, and S.A. Wolf, Eds., American Institute of Physics, New York, 1978 p. 364.
2. M.F. Millea, A.H. Silver, and L.D. Flesner, Thin Solid Films, 56, 253 (1979).
3. T.D. Clark, R.J. Prance, and A.D.C Grassie, J. Appl. Phys. 51, 2736 (1980).
4. D.J. Frank, M.J. Brady, and A. Davidson, IEEE Trans. on Mag., MAG-21, 721 (1985).
5. T. Nishino, M. Miyake, Y. Harada, and U. Kawabe, IEEE Electron Dev. Lett. EDL-6, 297 (1985).
6. H. Takayanagi and T Kawakami, Phys. Rev. Lett. 54, 2449 (1985).
7. T. Kawakami and H. Takayanagi, Appl. Phys. Lett. 46, 92 (1985).
8. A.W. Kleinsasser, T.N. Jackson, G.D. Pettit, H. Schmid, J.M. Woodall, amd D.P. Kearn, submitted to Appl. Phys. Lett. (1986).
9. T. Kobayashi, H. Sakai, Y. Kurita, M. Tonouchi, and M. Okada, Japanese Jour. Appl. Phys. 25, 402 (1986).
10. H. Tamura, S. Hasuo, and T. Yamaoka, Japanese Jour. Appl. Phys. 24, L709 (1985).
11. M.J. Brady and A. Davidson, Rev. Sci. Instrum. 56, 1459 (1985).
12. P.A. Moskowitz, S.M. Faris, and A. Davidson, IEEE Trans. on Mag. MAG-19, 503 (1983).
13. S.M. Sze Physics of Semiconductor Devices Wiley-Interscience, New York, 1969, p. 421.