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GaAs–GaAlAs HETEROJUNCTION TRANSISTOR FOR HIGH FREQUENCY OPERATION

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Abstract—A bipolar transistor structure is proposed having application for either high frequency operation or integration with certain types of light emitting devices. The structure involves liquid phase epitaxially grown layers of GaAs for the collector and base regions, and of $Ga_{1-x}Al_xAs$ for the heterojunction emitter. The high frequency potential of this device results primarily from the high electron mobility in GaAs and the ability to heavily dope the base region with slowly diffusing acceptors. The $Ga_{1-x}Al_xAs$ emitter region provides a favorable injection efficiency and, because it is etched preferentially relative to GaAs, access to the base layer for making contact. Transistor action with d.c. common emitter current gains of 25 have been thus far observed. Calculations of the high speed capability of this transistor are presented.

NOTATION

x	mole fraction of AlAs
β	d.c. common emitter current gain
d	base width
W	base stripe width
τ_b	base transit time
e	charge of the electron
k	Boltzmann's constant
T	temperature
μ_e, μ_h	electron and hole mobilities
R_s	base sheet resistance
N_{Ab}	acceptor concentration in the base region
N_D	donor concentration
ΔV	potential barrier of collector junction
C_c, A	collector junction capacitance and area
ϵ_0	permittivity of free space
κ	relative dielectric constant
R_b	base resistance
N_{De}	donor concentration in the emitter region
D_n, D_p	electron and hole diffusion constants
L_p	diffusion length of holes
τ_s	switching time
C_L, R_L	load capacitance and resistance

INTRODUCTION

AFTER more than a decade of rapid progress, Si and Ge bipolar transistors appear to be approaching their optimum high-frequency performance as determined by the semiconductor materials properties and the present transistor fabrication technologies. In this paper we will describe a new bipolar heterojunction transistor structure and the technique for its fabrication. The structure is based on the GaAs–$Ga_{1-x}Al_xAs$ system and offers advantages over Si and Ge bipolar transistors in terms of most of the characteristics that contribute to a high frequency capability. These advantages result partly from the physical and chemical properties of GaAs and $Ga_{1-x}Al_xAs$, and partly from the unique approach used in the fabrication of the transistor structure. Some estimates of the high frequency characteristics which might be expected from such a device will also be presented.

In addition to its use in high-frequency applications, the GaAs–$Ga_{1-x}Al_xAs$ structure described here could be integrated with other GaAs based optical devices, for example with GaAs–$Ga_{1-x}Al_x$-As light emitting arrays. The ability to integrate transistors and light emitting devices on a common substrate offers several potential advantages including greater simplicity, smaller size, and lower cost.

PROPOSED DEVICE STRUCTURE

A schematic representation of our proposed device structure is shown in Fig. 1. An n-GaAs collector layer, a p-GaAs base layer, and an n-$Ga_{1-x}Al_xAs$ emitter layer are grown in sequence on an n^+-GaAs substrate [Fig. 1(a)]. Using a recently developed liquid phase epitaxial (LPE) growth technique[1], the layers are grown from separate melts while maintaining the growing solid–liquid interface. The technique allows the controlled growth of uniformly doped layers as thin as 1000 Å.

The device is fabricated by first depositing onto

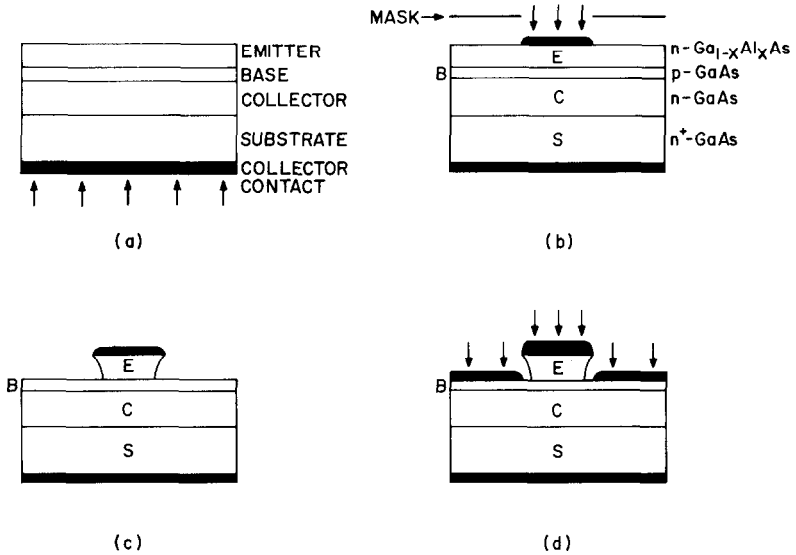

Fig. 1. Schematic drawing of the proposed transistor structure at different steps in its fabrication. (a) LPE grown layered structure with deposited collector contact. (b) Deposition of emitter contact which serves as a mask when unprotected portions of the emitter are removed (c) by a selective etch. During the vacuum deposition of the base contact (d) the undercut emitter contact provides a self registered separation between the base contact and the emitter junction.

a substrate a large area ohmic contact which serves as the collector contact [Fig. 1(a)]. Next the emitter contact is deposited through a metal mask [Fig. 1(b)]. This contact serves also to protect the emitter region when the unwanted part of the emitter layer is removed by a selective etching technique [Fig. 1(c)]. Following that, the revealed portions of the base layer are contacted by a final metal deposition [Fig. 1(d)].

ADVANTAGES OF PROPOSED STRUCTURE

The device structure shown in Fig. 1 offers several advantages for high-frequency performance. The most important of these advantages results from being able to make a thin, highly-doped p-type base region of GaAs. As has been widely appreciated[2] the relatively high electron mobility in GaAs contributes to a very low minority carrier base transit time (in an n–p–n transistor). Now, however, using LPE one can grow a more heavily doped base region with a base resistance which is lower than is possible by diffusion or by gaseous phase epitaxy techniques. The growth of the base by LPE also allows the use of slowly diffusing dopants and therefore provides the sharply defined impurity profile necessary for a thin base region.

The $Ga_xAl_{1-x}As$ region has a very close lattice match[3] with GaAs with which it forms a heterojunction emitter. Since $Ga_xAl_{1-x}As$ has a larger band gap than does GaAs, the energy barrier restricting the injection of holes from the base into the emitter will be greater than that restricting the injection of electrons from emitter to base. As has been previously recognized[4] this should result in a favorable injection efficiency and contribute to a high value of current gain. Because of the high base doping in our structure it is doubtful that a suitable injection efficiency could be achieved without a heterojunction emitter.

Other heterojunction emitters that have been previously investigated and which also have a very good lattice match are GaAs–Ge[5] and ZnSe–Ge[6]. In both of these junctions, however, there exists the likelihood of cross-doping which can considerably complicate the control of the doping profile in the region of the junction. No cross-doping can occur in a $Ga_{1-x}Al_xAs$–GaAs heterojunction, however, because Ga and Al are isoelectronic. Furthermore, since the collector, base, and emitter layers are grown in situ, the present LPE growth technique eliminates surface contamination at the heterojunction interface.

The properties of $Ga_xAl_{1-x}As$ provide several other attractive features which simplify the fabri-

cation and improve the performance of the proposed device. One feature is that $Ga_xAl_{1-x}As$ can be etched preferentially with respect to GaAs. This facilitates removal of part of the $Ga_xAl_{1-x}As$ layer in order to make contact to the GaAs base region. The importance of this capability should not be dismissed since much of the effort of Dismukes, Dean and Nuese[7] on vapor grown GaAs transistors involved investigation of techniques for making contact to the base. Another type of base contact could be provided by a diffusion through part of the emitter area to the base, although this method would probably result in both a decreased injection efficiency and a smearing of the impurity profile.

The etching properties of $Ga_xAl_{1-x}As$ can also be utilized to obtain a considerable reduction in the collector junction area. This reduction results because it is possible to automatically register the position of the base contact relative to that of the emitter and thereby reduce the area resulting from the separation between the emitter–base junction and the base contact. The etchant removing the unwanted portion of the $Ga_xAl_{1-x}As$ is allowed to undercut the emitter contact, thus providing a small but even separation between the edges of the emitter junction and a vacuum evaporated base contact [Fig. 1(d)].

PRELIMINARY RESULTS

Several studies were initiated to determine the feasibility of achieving devices with the desired properties. These studies have concentrated on the critical problems of growing layered structures having the desired layer thicknesses and doping levels, and etching studies of the $Ga_{1-x}Al_xAs$ emitter masked with relatively large area emitter contacts.

In Fig. 2 we show a phase contrast photomicrograph of one of our layered structures. After this structure was grown on an n-type (100) GaAs substrate it was cleaved on a (110) plane parallel to the growth direction and then etched to reveal the layers. The line nearest the bottom of the figure is the substrate–collector interface. The dark line above it is the collector–base interface. The next contrast boundary $\sim 1\ \mu m$ above the base–collector boundary is the emitter–base interface. The composition of the $2\ \mu m$ thick emitter layer is $Ga_{1-x}Al_xAs$ with $x = 0.5 \pm 0.05$.

The dopants used were Sn in the collector and emitter, and Ge in the base region. Since Sn and Ge are non-volatile, cross contamination between the different melts is minimized and thus better doping control is achieved. In addition, Ge has a much smaller diffusion coefficient than volatile group II dopants such as Zn and Cd.

Doping levels of the collector and base regions of the structure shown in Fig. 2 were determined from Hall effect and plasma resonance measurements. This sample had a collector electron concentration of $4 \times 10^{17}\ cm^{-3}$ and a base hole concentration of $1\text{–}2 \times 10^{18}\ cm^{-3}$. The electron concentration of the emitter could not be established, but an estimate based on behavior similar to Sn doping in GaAs would put the value at approximately $5 \times 10^{17}\ cm^{-3}$.

One of the requirements for the fabrication of our proposed transistor is the ability to selectively etch away the emitter layer to expose the base for contacting. We have found that HCl acid will dissolve $Ga_{1-x}Al_xAs$ if $x > 0.3$. The rate of dissolution increases with increasing x, temperature, and concentration of the HCl. In the time required to dissolve a $10\ \mu m$ thick $Ga_{1-x}Al_xAs$ layer the dissolution of pure GaAs was $\ll 0.1\ \mu m$. Thus, the emitter material can be removed without disturbing the GaAs base and without having to strictly monitor the etching process. Furthermore, we found that the Au–Ge eutectic alloy forms a good ohmic contact to n-type $Ga_{1-x}Al_xAs$ and is very resistant to attack by the HCl. Thus, it provides a suitable mask for protecting the desired emitter areas during selective etching.

In order to determine whether or not acceptable current gains could be obtained from the proposed transistor structure, initial test devices have been made and their common emitter and common base characteristics measured. Partly because these devices had relatively large emitter areas ($3 \times 10^{-4}\ cm^2$) and partly because of contact resistance to the ultrasonically bonded leads, low emitter current densities were used. The I–V characteristics for low values of V_{EC} were typical of transistors except for some distortion produced by the emitter contact resistance. In spite of the large emitter areas the values of I_{Co} were respectably low, corresponding to a current density of $\sim 1\ A/cm^2$. Beyond $V_{EC} \sim 4V$ there was a gradual rise in I_c indicating some multiplication in the collector junction. The d.c. current gain was a rapidly increasing function of gain and values of the common emitter gain, β, of 25 were observed. We expect to be able to obtain higher values of β with smaller area emitters. Future

work will include photolithographic processing to obtain devices with smaller junction areas which will also be more suitable for high frequency operation.

CALCULATED PERFORMANCE

Our results to date have shown that reasonable values of β can be obtained from heterojunction transistors made from GaAs and $Ga_{1-x}Al_xAs$. A better idea of the high frequency performance potential of such devices can be obtained, however, if we calculate some of the important parameters related to high frequency operation for a structure with dimensions typical of a modern high speed transistor. We shall assume a 1200 Å base width, d, and an emitter and two base contact stripes each of length 12.5 μm (0.5 mil) and of width, W, equal to 2.5 μm (0.1 mil). Any areas beyond the sides and ends of the base contact stripes may, after suitable masking, be removed by an appropriate etch. Allowing a small separation of 0.5 μm between the self registered emitter and base contact stripes, we obtain a collector area of $12.5 \times 8.5\ \mu m^2$.

Assuming an acceptor doping $N_{ab} = 3 \times 10^{18}\ cm^{-3}$ in the base region, the majority and minority carrier mobilities are[8, 9] approximately 130 cm^2/V-sec and 2300 cm^2/V-sec respectively. The base transit time at room temperature would be

$$\tau_b \sim \frac{d^2 e}{2\mu_e kT} = 1.2\ \text{psec}.$$

The base sheet resistance is given by

$$R_S = \frac{1}{dN_{Ab} e \mu_h} = 1330\ \Omega/\square.$$

The majority carriers must travel 0.5 μm between the base contact and the emitter junction and an average distance of $1/4W = 0.625\ \mu$m under the emitter. Since the sides of the emitter total 25 μm, the base resistance is $R_b = 60\ \Omega$. For a collector doping of $N_D = 3 \times 10^{16}\ cm^{-3}$ and with an average built in potential difference, ΔV, of 1 V, the collector capacitance per unit area would be approximately

$$C_c/A = \left(\frac{8\epsilon_0 \kappa N_D}{2\Delta V}\right)^{1/2} = 5.15 \times 10^{-8}\ F/cm^2.$$

For a $12.5 \times 8.5\ \mu m^2$ area, $C_c = 5.5 \times 10^{-2}$ pF, yielding an $R_b C_c$ product of 3.3 psec.

We have assumed a fairly light collector doping ($3 \times 10^{16}\ cm^{-3}$) which helps in obtaining a low value of C_c. It has been reasonable to assume this low a value of collector doping because:

(1) the high electron mobility in the collector ($> 5000\ cm^2$/V-sec) will help furnish a low series collector resistance, and
(2) the high doping in the base region will prevent any significant base stretching[10] at high current densities. There will be a greater shift of the high field region into the collector region due to this effect, but this is much less important due to the relatively high drift velocities of electrons in this region.

The injection efficiency is increased to acceptably high values by using a heterojunction emitter. Without this emitter the d.c. current gain estimated from the emitter efficiency would have been

$$\beta = \frac{N_{De} D_n / d}{N_{Ab} D_p / L_p} = 17,$$

assuming an emitter doping of $N_{De} = 3 \times 10^{17}\ cm^{-3}$, a hole diffusion length, L_p, of 2 μm and a hole diffusion constant of 5 cm^2-sec.

Using a $Ga_xAl_{1-x}As$ emitter with a band gap only 0.1 eV greater than that of GaAs will increase β by a factor of $\exp(0.125\ e/kT) = 45$ at 300°K to a value greater than 700.

Estimates of the high speed performance can now be made using calculated values of τ_b, R_b and C_c. The gain-bandwidth product $f_T = 1/2\pi\tau_b$ would be 130 GHz. The switching time can be estimated using Ashar's linearized analysis[11] of a two transistor current switch as modified by Dumke[12]. If R_L and C_L are the load resistance and capacitance of the circuit, then the switching time may be written as

$$\tau_s = \tfrac{5}{2} R_b C_c + \frac{R_b}{R_L}\tau_b + (3C_c + C_L)R_L.$$

Taking $R_L = 50\ \Omega$ and considering the unloaded case, $C_L = 0$, we obtain a switching time of 18 psec, roughly a factor of 5 or 8 faster than that which might be realized from the current post alloy diffused Ge or double diffused Si technologies respectively.

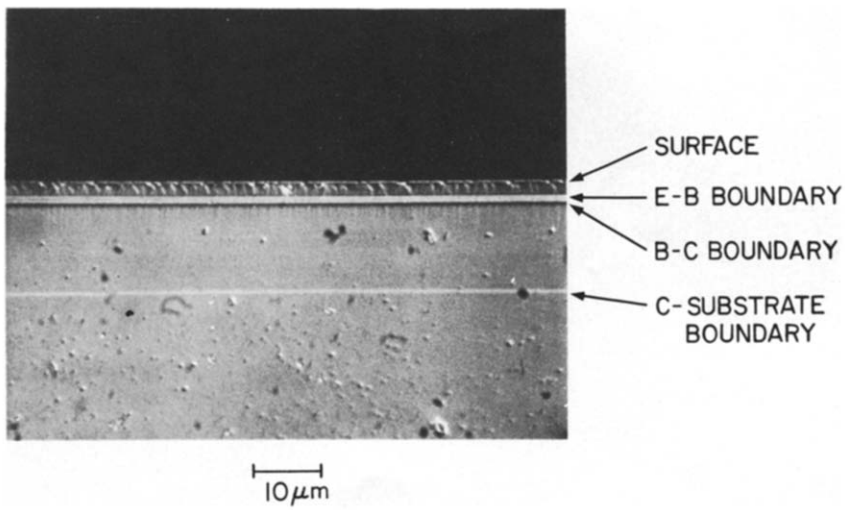

Fig. 2. Photomicrograph of a GaAs–$Ga_{1-x}Al_xAs$ layered structure grown for transistor fabrication. The different layers are described in the text.

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CONCLUSIONS

We have proposed a transistor structure and a way of making it which should result in outstanding high frequency performance. Some of the ideas incorporated here, such as the high electron mobility afforded by GaAs and the use of a heterojunction emitter, are of course well known. The ability to make thin, heavily doped base regions in GaAs and to reveal and contact these base regions by selective etching techniques however now provides the complementary technology necessary to make a successful device. Preliminary development has demonstrated the feasibility of the proposed transistor, and calculations of its expected performance indicate its superiority to the present Si and Ge high-frequency bipolar technologies.

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