Effective barrier heights of mixed phase contacts: Size effects

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Computer simulations of mixed phase Schottky contacts have been performed to gain insight into the effects of lateral dimensions upon device behavior. As expected, lateral dimensions comparable to the Debye length of the semiconductor result in strong modification of the device characteristics that would result from independent, parallel diodes. We suggest that such effects can play a role in most experimentally obtained contacts. Current models of Schottky barrier formation typically invoke kinetics-limited chemical interactions at the metal-semiconductor interface; such effects are unlikely to be laterally uniform over macroscopic dimensions, and may well provide strong sensitivity to seemingly minor variations in preparation techniques used by different groups. We demonstrate that mixed phase contacts, with size effects, can affect ideality factors, and can also cause disagreement between *C-V* and *I-V* barrier heights.

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The literature currently abounds with experimental studies of Schottky barrier heights of various metals upon many semiconductors. Unfortunately, barriers determined by *C-V* studies are often larger than barriers determined by *I-V* studies.[1] Furthermore, barriers deduced via identical techniques for apparently comparable preparation procedures are not always reproduced from group to group.[2] A possible explanation for such effects is simply that many/most contacts experimentally achieved are in fact multiphase; these different barrier height regions could result from variations in the metallurgical reactions assumed by many current models of Schottky barrier energetics.[3-6] The different barrier heights measured by different techniques follow directly from the functional form of the relevant probes (e.g., *I-V* would heavily weight a low barrier region).[7] A lack of reproducibility would follow from kinetic aspects of the relevant metallurgical interactions.

A recent publication[7] discusses the functional form for *I-V* and *C-V* "effective" barrier heights from mixed-phase contacts *isolated* from one another. The authors demonstrated that barrier height and area ratio of the two phases totally determined the effective barrier heights. These results directly apply to mixed-phase contacts only if the linear dimensions of all contacts are large compared to the Debye length of the substrate (i.e., $\gg 0.1\ \mu$ for 10^{15} carriers/cm^3 *n*-silicon). The reason for this limitation is that the analysis of Ref. 7 neglected the constraints of continuous fields within the semiconductor; as noted in this reference, such neglect is unimportant for large contacts. At small sizes, however, this requirement can vastly alter the space-charge region under the contacts, and therefore alter the observed transport and band bending. In this letter we examine the effects of contact dimensions upon transport studies to infer effective barrier heights for truly mixed-phase contacts of varying dimensions but fixed area ratios.

The calculations were performed using FIELDAY, a finite element device analysis program[8,9] that simultaneously solves Poisson's equation and the current continuity equations in two dimensions; the calculations were performed both at equilibrium and away from equilibrium, thereby permitting direct simulation of the common experimental probes used to determine Schottky barrier heights.

In Table I we show the effects of varying size upon mixed-phase Schottky barriers of fixed area ratio, where a 0.2-V contact with $\approx 1/8$ the total area is imbedded in a large barrier (0.8 V) region. The total contact width is shown in the second column: the 0.2-V barrier contact has a width of 1/8 that dimension, the 0.8-V contact has a width of 5/6 that dimension, and there is a gap of 1/24 the total width. The program is told that the substrate has silicon parameters and is $2\ \mu$ thick, where it is contacted by an ohmic charge neutrality-defined contact. This program generates boundary con-

TABLE I. Barrier heights ϕ_{bn}, doping N_D, and ideality *n*, as extracted by standard techniques from computer-simulated current and charge response to bias variations. The contacts denoted by sizes contain a 0.8-V barrier as 5/6 the total area, and a 0.2-V contact as 1/8 the total area. The width of the 0.2-V contact is 1/4 times the size shown in the second column. The *I-V* results are two point fits using forward bias of 0.05 and 0.1 V (0.1 and 0.2V).

MATERIAL		C-V		I-V	
SYMBOL	SIZE	ϕ_{bn} (V)	N_D (cm^{-3})	ϕ_{bn} (V)	n
+	4μ	0.906	9.85E14	0.395 (0.378)	2.76 (5.41)
×	2μ	0.756	8.46E14	0.4 (0.383)	2.6 (4.74)
□	1μ	0.63	8.24E14	0.447 (0.426)	1.78 (2.79)
○	$1/2\mu$	0.709	9.93E14	0.526 (0.508)	1.28 (1.66)
Δ	$1/4\mu$	0.713	1.00E15	0.587 (0.575)	1.14 (1.32)
*	$1/8\mu$	0.713	1.00E15	0.618 (0.625)	1.28 (1.18)
			SINGLE PHASE		
0.8 Barr.		0.800	1.00E15	0.800 (0.793)	0.94 (1.00)
0.2 Barr.		-5.26	-2.27E15	0.352 (0.335)	2.83 (5.5)

ditions by assuming that the edges of the defined contact are mirror-symmetry lines; this means that the "true" width of the low and high barrier regions is twice that inferred above (but the area ratios are, of course, fixed). The program further assumes zero spatial variation in the third dimension (i.e., length is assumed infinite). The table shows the effects of this mixed-phase contact upon experimental determinations of barrier height by the common techniques of (log I) vs *V* and by $(1/C^2)$ vs *V*. For comparison, we also show the results obtained by the computer for the low and high barrier contacts by themselves, i.e., as single-phase contacts; clearly, *C*-*V* studies of the accumulated low barrier interface would not generate a believable barrier height.

Clearly, the absolute size of the two regions strongly affects the experimentally determined barrier height. As the low barrier height region width gets smaller, it is more effectively "pinched off" by the large barrier contact, leading to a larger barrier. For comparison, the analytical solution of Ohdomari and Tu[7] (who neglected this effect) gives an *I*-*V* barrier of 0.249 V, and cannot give a *C*-*V* result, since the 0.2-V barrier accumulates the surface. Their result would be the same for all sizes shown, since they did not address size effects.

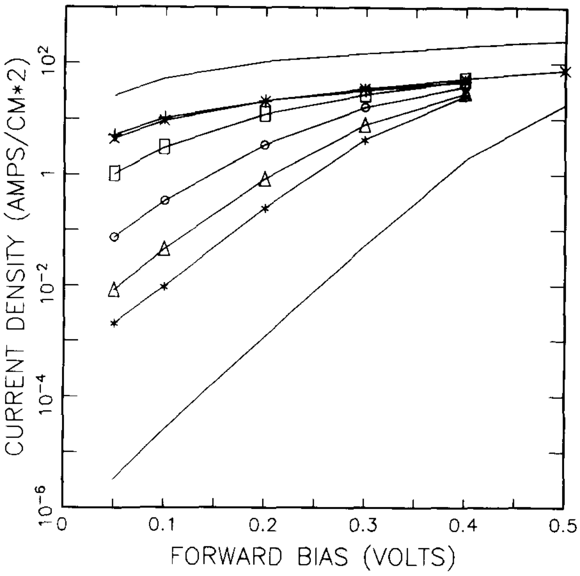

FIG. 2. Logarithm of current density vs forward bias for contacts as discussed in Fig. 1.

The figures show the calculated current and $(1/C^2)$ for the various sizes at various biases; the symbols denote sizes as shown in Table 1. Figure 1 shows the current density versus bias, Fig. 2 shows the logarithm of the current density versus forward bias, and Fig. 3 shows the values of $(1/C^2)$ under reverse bias. The points shown in Figs. 2 and 3 were used in the standard procedures of extracting barrier height from experimental data; the capacitance results used all the points, whereas the *I*-*V* results used only the first two (or the second and third), since resistive effects are commonly used to discard data points in such measurements. Clearly, the capacitance data alone provides no "warnings" concerning the mixed-phase nature of the contact being studied. The *I*-*V* data, especially that from the larger contacts, provides warnings of a resistive effect (apparently the cause of the large idealities sometimes inferred), but many of these contacts would appear to be "normal," single-phase contacts to both techniques. It would appear that transport data from a particular contact would not always give any warning of mixed phases other than a discrepancy between *C*-*V* and *I*-*V* derived barrier heights. Furthermore, a mixed-phase contact can provide strong rectification even if the minority phase is an ohmic contact.[4,10]

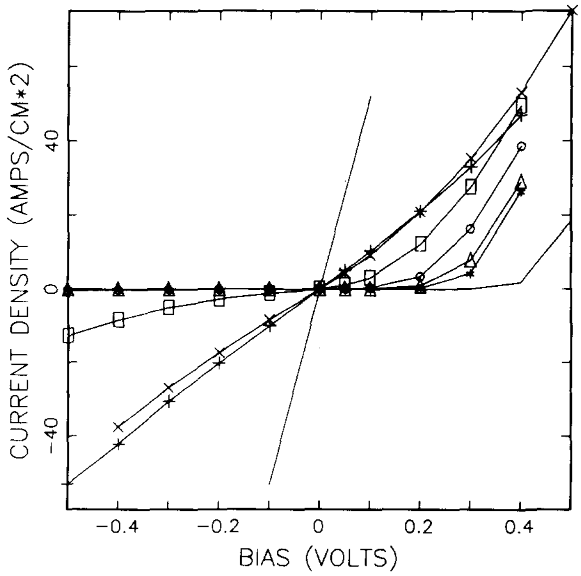

FIG. 1. Current density vs applied voltage for contacts of varying sizes (see text). Symbols denote sizes as indicated in Table I; lines refer to single-phase contacts of 0.8- and 0.2-V barrier heights.

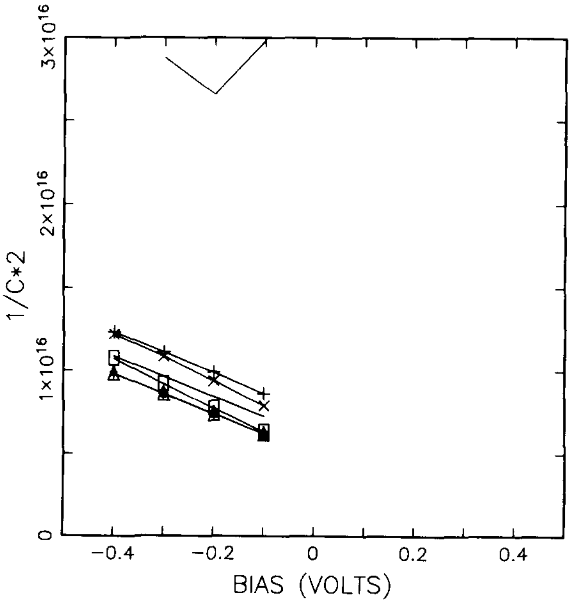

FIG. 3. Inverse capacitance vs reverse bias of contacts discussed in Fig. 1 caption (capacitance units are farads/cm^2).

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Planarization of patterned surfaces by ion beam erosion

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The angular dependence of ion beam erosion has been utilized to achieve planarization of patterned surfaces. Deviation from planarity of < 500 Å has been demonstrated on planarized SiO_2 covered patterned Si surfaces with 1.5-μm-deep recesses. The technique should be applicable to a wide variety of materials with different physical, chemical, optical, and electrical properties, and should be particularly useful in very high speed integrated circuit development.

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The existence of topographic steps on patterned surfaces presents several obstacles to the achievement of higher speed and higher packing density of integrated circuit devices. Minimum feature size of lithographic techniques is severely restricted by resolution and linewidth control limitations associated with the presence of steps; poor coverage of stepped surfaces leads to unreliable metallization interconnections, and vertical stacking of integrated circuits is almost certainly prohibited by a stepped topography. Minimum feature size and packing density are also limited by the lateral oxidation characteristic of local oxide formation on patterned surfaces.[1] These limitations would be removed if the recesses on a patterned surface were filled with an inert material and the surface planarized prior to subsequent processing operations. Planarizing may be accomplished by the technique shown schematically in Fig. 1. A patterned surface is covered by a film of inert material *B* followed by a film of liquidlike material *C* so that the top surface of *C* is planar [Fig. 1(b)]. If *C* and excess material *B* are removed by plasma etching,[2] sputter etching,[3] or reactive ion etching, a planar surface will be preserved throughout the etching process if the etch rates of *B* and *C* at normal incidence are identical [$\phi = 0°$ in Fig. 1(c)]. In general, the normal incidence etch rates of *B* and *C* are different and the applicability of these etching techniques to planarizing is severely limited. However, ion beam milling provides freedom to choose a nonnormal angle of incidence for the sputtering beam. For SiO_2 (material *B*) and AZ-1350 photoresist (material *C*), for example, the ion beam erosion rates at an angle of incidence of 59° are equal (Fig. 2), and at this angle a planar surface should be

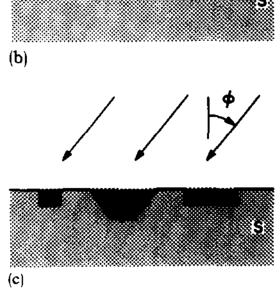

FIG. 1. Schematic of planarizing technique. (a) Patterned surface with maximum recess depth *d*. (b) Patterned surface covered by a film of inert material *B* and planarizing film *C*. To obtain a planarized surface with recesses completely filled with *B* requires that the minimum thickness of *B* satisfy $t > d$. (c) Surface planarized by erosion at angle of incidence ϕ where the erosion rates of *B* and *C* are identical.

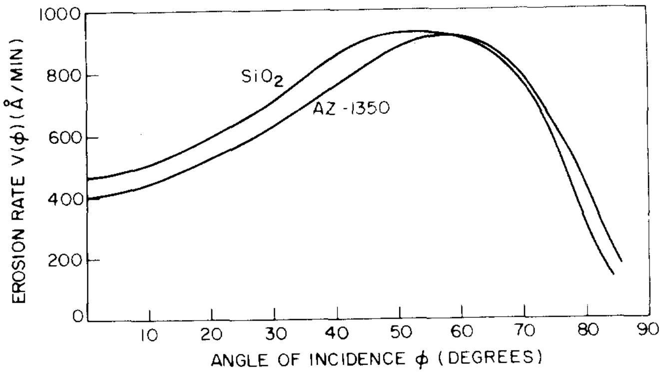

FIG. 2. Angular dependence of the erosion rate for SiO_2 and AZ-1350 photoresist under argon ion beam milling [normalized data from Somekh and Casey (see Ref. 5) and Bollinger (see Ref. 6)].