Studies of GaAs–oxide interfaces with and without Si interlayer

J. L. Freeouf, D. A. Buchanan,[a] S. L. Wright, T. N. Jackson, J. Batey, B. Robinson, A. Callegari, A. Paccagnella, and J. M. Woodall
IBM Research, Yorktown Heights, New York 10598

(Received 31 January 1990; accepted 28 March 1990)

We have studied the properties of metal–oxide–semiconductor structures fabricated by plasma enhanced chemical vapor deposition of SiO_2 upon GaAs substrates. We have characterized the dependence of these properties upon the presence of a silicon interlayer, the type and the degree of misorientation of the substrate, and the type of plasma enhancement. We conclude that the presence of a silicon interlayer is beneficial for *n*-type GaAs if the oxide is deposited by a remote plasma technique. For such oxides on *n*-type GaAs coated with silicon, integration of the quasi-static capacitance curve suggests a band-bending range of 0.6–0.9 V. Also for these samples, we observe a hysteresis of order 0.6 V, and shifts of only 0.2 V in the midpoint of the rise from minimum to maximum capacitance upon changing frequency from 10 to 200 kHz. The benefits of using a silicon interlayer with a direct plasma deposited SiO_2 film are less evident. It is assumed that much of the improvement of these results arises not from a large reduction of the interface density but rather from a shift of the spectrum towards the conduction band edge. This appears evident from the improvement on *n*-type samples coincident with a degradation on *p*-type samples. The total band bending change derived from the integral from the quasi-static capcitance–voltage curves is less sensitive to this interlayer than is the frequency dispersion.

I. INTRODUCTION

The history of GaAs-based metal–oxide–semiconductor (MOS) structures is a long one.[1] The advantages of the large band gap and high electron mobility of GaAs have long been recognized, and many efforts to fabricate MOS transistors have been pursued. Enhancement-,[2] depletion-,[3,4] and inversion-[5,6] mode field effect transistors (FETs) have been fabricated, but none exhibit optimal operating characteristics. The dominant limitations[1] have been the high degree of Fermi level pinning at the interface—a well-known problem with most interfaces with GaAs—and low-quality deposited and/or grown insulators. Recent studies of GaAs Schottky barrier formation have found a few instances of decreased Fermi level pinning.[7] A recent attempt to understand these results suggested that step density and surface reconstruction may both be connected to this result.[8]

Recent work by several groups[9–11] has achieved high quality insulator deposition at low temperatures by an enhanced chemical vapor deposition (CVD), typically of SiO_2. The resulting oxide can be of quite high quality, often exhibiting breakdown strengths (on GaAs) within a factor of 2 of that achieved on Si substrates, and sufficiently uniform and trap free as to exhibit low leakage currents for oxide thickness's of order 200 Å.[4,6] Several groups have further suggested improvements in the interface quality associated with the deposition of a thin silicon interlayer[4,6,11] onto the as-grown GaAs surface. We previously established[9] that under direct plasma enhanced CVD conditions, the presence of the silicon interlayer had little or no impact upon the sample characteristics after a standard 600 °C post-oxide anneal (POA). We used spectroscopic ellipsometry to establish that, under our conditions, the silicon interlayer was entirely oxidized prior to the deposition of the CVD oxide.

Defining exactly how "good" these interfaces are can be a bit tricky. The density of interface states is rather difficult to infer from such structures, but numbers as low as 4×10^{11} cm^{-2} have been quoted recently.[10] These numbers may suggest a nearly Si-quality interface; such is not the case, since both hysteresis and frequency dispersion are clearly occurring in these systems.

In the present work we have studied the electrical characteristics of MOS structures as a function of oxide deposition class, the presence or absence of a silicon interlayer, and the orientation of the GaAs wafer (the step density is the intended variable). Anneal temperature and ambient are essential aspects of any such study and were also addressed. The results suggest that the silicon interlayer is an important adjunct to the process only for a remote plasma CVD (not a direct plasma) and only improves the capacitance–voltage (C–V) properties on *n*-type GaAs. Furthermore, our results suggest that the inferred improvement largely concerns which portion of the band gap is accessible under applied bias. The total band bending change [derived from the integral of the quasistatic (QS) C–V curve] is less sensitive to this interlayer.

II. EXPERIMENT

The Si and GaAs layers were grown by molecular-beam epitaxy (MBE) on n^+ or p^+ substrates in a Varian GEN II MBE system. All surfaces are (100) oriented, and most are the nominal 2° off axis (towards the nearest ⟨110⟩) commonly used in MBE. Two samples are oriented within 0.5° of the (100) axis and will be discussed separately. The silicon is deposited from a resistively heated filament source as a single crystal layer, judging from the reflection high-energy electron diffraction (RHEED) pattern observed following the deposition. Both RHEED and Auger results strongly suggest total coverage of the GaAs by the thin silicon layer, but do not establish the total thickness of the layer. We estimate this thickness between 10–30 Å.

 0734-211X/90/040860-07$01.00 © 1990 American Vacuum Society

Following sample growth, the samples were removed from the vacuum system, separated into pieces as needed, and carried to the oxide CVD systems under study. Both systems involve plasma enhanced CVD of SiO_2 from feed gases of SiH_4 and N_2O. In one system, the plasma region encompasses the sample[12] and all gases (which we refer to as the "direct" plasma). In the other, the plasma region is remote from the sample, and only N_2O is exposed to the plasma[13] while the SiH_4 is injected downstream from the plasma. This system we refer to as the "remote" plasma system. The remote plasma depositions were performed at a deposition temperature of 325 °C, and the direct plasma depositions were performed at 275 °C. A second direct plasma CVD system was used for a few samples to sputter deposit a thin silicon layer followed immediately by an oxide deposition.

Following oxide deposition, the samples were further divided and subjected to a matrix of post oxide anneals in nitrogen or forming gas ($\sim 5\%$ H_2 in argon), deposition of 3000 Å Al through a shadow mask providing 8-mil diameter dots, followed by a Au–Ge based back contact deposition and a 30 min post metalization anneal at 300 to 400 °C in forming gas.

The oxides and their interfaces were characterized by an ellipsometric system described previously.[14,15] Several samples were studied prior to annealing, and a few were also studied after the post-oxide anneal. The analysis was performed, as usual, by letting a nonlinear least squares minimization routine optimize the agreement between a multilayer model of the sample and the experimentally obtained data.

Capacitance–voltage (C–V) data were taken at various frequencies ranging from 10 to 200 kHz using a Hewlett Packard 4275A LCR meter and an HP 4140B as a capacitance meter and ramped voltage supply, respectively. Voltage ramp rates were either 100 or 200 mV/s. However, no significant differences in hysteresis or frequency dispersion were found for rates as low as 25 mV/s. Quasistatic C–V data were taken using either a ramped or a stepped supply voltage. In the former, a slow ramp was applied, and from the displacement current the capacitance is derived from $I = C(dV/dt)$. In the stepped voltage technique, the voltage is incremented in small steps, and the charge measured using a Keithley 617 electrometer. The capacitance, in this case, is derived using $C = (dQ/dV)$. For some samples, significant leakage currents were observed. In these cases, the step voltage technique was used since it is less susceptible to errors incurred by gate oxide leakage.

III. RESULTS

The spectroscopic ellipsometry data provides information about the purity of the deposited oxide and the amount of unoxidized silicon at the interface. In all cases we have SiO_2 on GaAs. The interface determined in this fashion is the native oxide of GaAs mixed with GaAs for samples without a deposited Si interlayer, and SiO_2 mixed with GaAs for samples with a deposited Si interlayer. (The mixture is a means of simulating interface roughness.)

The only observation of unoxidized silicon is for the samples where the silicon was deposited in the CVD system rather than in the MBE system. Raman scattering studies of this silicon-containing sample after a 600 °C anneal in N_2 for 30 min found virtually no indication of fourfold coordinated silicon, suggesting that the interface layer is some form of suboxide.

The electrical measurements offered more variety in the results, although the reproducibility is concomitantly weakened. As shown in Tables I and II, hysteresis was observed to vary from 3 to 0.6 V, frequency dispersion on n-type GaAs varied from shifts of over 3 V down to as low as 0.2 V, and integrating the QS curve led to inferred band bending changes from 0.2 to 0.9 V. This much variation suggests that we are able to modify aspects of the sample affecting these properties. We must therefore examine which variables lead to which types of electrical results. First, however, we discuss the electrical results more generally, to establish the kinds of results obtained, and the questions concerning interpretation of such results.

TABLE I. A summary of the electrical results obtained from capacitance–voltage studies at room temperature of GaAs-based MOS structures. The samples were nominally on axis and were within 0.5° of (100) n-type GaAs. Tabulated are the anneal temperature and ambient [N_2 or forming gas (FG) for 30 min], the integral of the quasi-static curve, the hysteresis of the 10 kHz curve, and the shift in the midpoint of the C_{min} to C_{max} between the 10 kHz curve and the 100 kHz curve. All oxides were deposited using the direct plasma deposition technique.

Silicon interlayer	Anneal	QS integral (eV)	Hysteresis (10 kHz) (V)	Dispersion 10–100 kHz shift (V)
None	500 °C in FG	0.49	1.6	1.5
None	600 °C in N_2	0.52	2.0	0.7
None	625 °C in N_2	0.53	2.0	1.1
MBE	400 °C in FG	0.40	2.0	2.0
MBE	500 °C in FG	0.34	2.0	2.0
MBE	625 °C in FG	0.36	2.3	2.5
MBE	500 °C in N_2	0.39	2.0	2.0
MBE	625 °C in N_2	0.36	2.0	3.2

TABLE II. A summary of the electrical results are presented which were obtained from capacitance–voltage (C–V) studies at room temperature of GaAs-based MOS structures. The samples were 2° off-axis (100) GaAs. Tabulated are the oxide deposition type (direct or remote plasma), the silicon interlayer, anneal temperature and ambient, the integral of the quasi-static curve, the hysteresis of the 10 kHz curve, and the shift in the midpoint of the C_{min} to C_{max} between the 10 kHz curve and the 200 kHz curve.

Silicon interlayer	Substrate type	Oxide deposition	Anneal	QS integral (eV)	Hysteresis (10 kHz) (V)	Dispersion 10–100 kHz shift (V)
None	*n*	Direct	250 °C in FG	0.27	3.0	>8
None	*n*	Direct	600 °C in N_2	0.37	2.0	0.80
None	*n*	Remote	600 °C in N_2	0.35	1.4	0.80
None	*p*	Direct	250 °C in FG	0.36	2.0	0.8
None	*p*	Direct	600 °C in N_2	0.40	2.0	2.5
MBE	*n*	Direct	250 °C in FG	0.41	1.8	0.47
MBE	*n*	Direct	600 °C in N_2	0.60	1.6	0.5
MBE	*n*	Remote	600 °C in N_2	0.6 – 0.9	0.6	0.2
MBE	*p*	Direct	250 °C in FG	0.20	1.0	0.45
MBE	*p*	Direct	600 °C in N_2	0.33	1.6	0.90
MBE	*p*	Remote	600 °C in N_2	0.2	0.9	1.5
Sputtered	*n*	Direct	600 °C in N_2	0.40	0.9	2.3
Sputtered	*p*	Direct	600 °C in N_2	···	1.3	3.2

Figure 1(a) shows capacitance–voltage results for a sample without a silicon interlayer. This sample received a 600 °C anneal in N_2 after deposition of the SiO_2 film using a direct plasma system. It is clear that the swing from low ("depletion") capacitance to high ("accumulation") capacitance strongly depends upon the measurement temperature for a given frequency. Furthermore, the magnitude of the "low" capacitance increases as the temperature decreases. This latter effect has been observed in deliberately degraded silicon MOS structures[16] and indicates that the sample is not in thermodynamic equilibrium during the measurement. As noted previously,[9] the largest capacitance reached at low temperature is less than that reached at room temperature. This can be interpreted as being due to residual depletion in the semiconductor. One can therefore infer a residual band bending under such an assumption. For this sample, the residual band bending is 0.33 V.

Figure 1(b) shows C–V results for a sample with an MBE silicon layer for measurement temperature ranging from 123 to 293 K. This sample received a 400 °C anneal in forming gas after deposition of a direct plasma SiO_2 film. For this sample the inferred band bending is 0.45 eV. Comparing this figure to that of Fig. 1(a) it is evident that the sample without the silicon interlayer shows less frequency dispersion and less hysteresis for any given temperature. It should be noted that the anneals performed on the samples shown in Figs. 1(a) and 1(b) are different. However, both the heat treatments for the samples with and without a silicon interlayer have been optimized and as such represent the best anneal conditions for both cases. Both samples are *n*-GaAs grown on (100) substrates aligned within 0.5° of being on axis.

In some previously published work,[9] we found that 600 °C anneals optimized the C–V results for samples grown on the commonly used 2° misoriented substrates and coated by the direct plasma enhanced chemical vapor deposition (PECVD) oxide, regardless of whether or not they had a silicon interlayer. Capacitance–voltage results for samples with and without a silicon interlayer grown on such off-axis (2° misaligned) substrates and annealed at 600 °C are shown in Figs. 2(a) and 2(b), respectively. The differences in the characteristics of these samples with and without the silicon interlayer are much less striking than those shown in Figs. 1(a) and 1(b). In Fig. 2 we compare samples with and without a silicon interlayer at room temperature for two frequencies, 10 and 200 kHz. The sample with a silicon interlayer appears to demonstrate better C–V characteristics. However, these differences are not nearly as drastic as those in Fig. 1 which favored the sample without a silicon interlayer. For the sample in Fig. 2(b) we cooled to 173 K, and the maximum capacitance still was C_{ox}. Furthermore, the capacitance reached this value for an applied bias of about 3 V.

Results obtained from *p*-type samples are of particular interest, in part since *n*-channel inversion mode metal–oxide–semiconductor field effect transistor (MOSFETs) would be made on such material. In Fig. 3 we show results for one such sample at three temperatures. This sample contains a silicon interlayer and used the direct plasma oxide CVD approach. We clearly observe some anomalous effects with temperature, such as a more rapid approach to the accumulation high capacitance region at 223 than at 293 K. At still lower temperatures the C–V curves shift with temperature in a more normal fashion. Other anomalies in temperature dependence in *p*-GaAs MOS structures have previously been reported.[17,18]

Other workers[6,10] have deposited a silicon interlayer in a remote plasma CVD system (*in situ*) just prior to the SiO_2 deposition. In Figs. 4(a) and 4(b) C–V results are shown for

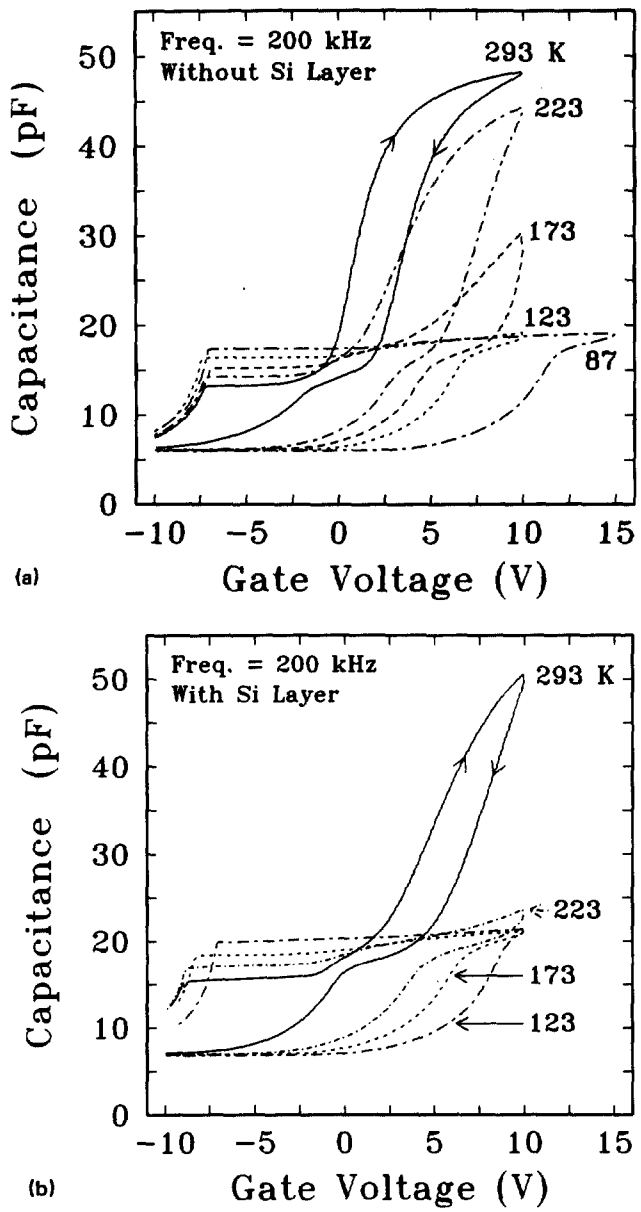

FIG. 1. 200 kHz C–V data for n-type GaAs oriented within 0.5° of the (100) axis. For (a) the sample has no silicon interlayer and has been annealed in N_2 for 30 min at 600 °C; for (b) the sample has a silicon interlayer and was annealed at only 400 °C in forming gas, which was the optimum anneal for this sample. The oxide was deposited by direct plasma enhanced chemical vapor deposition upon these air-exposed samples prior to their anneals. The results obtained at various temperatures (as labeled) are clearly varying, such that the increase from C_{min} to C_{max} is delayed as the temperature is lowered.

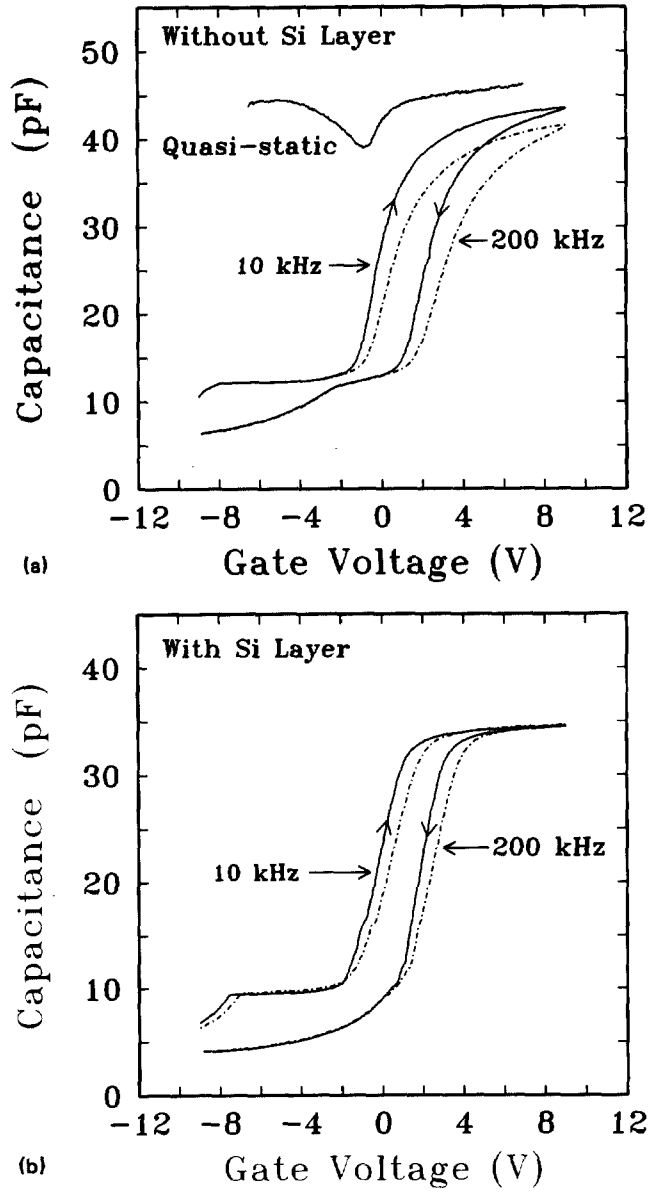

FIG. 2. 10 and 200 kHz C–V data for n-type GaAs oriented about 2° from the (100) axis. For (a) the sample has no silicon interlayer, while for (b) the sample has a silicon interlayer. The oxide was deposited by direct plasma enhanced chemical vapor deposition upon these air-exposed samples. Both samples were annealed in N_2 for 30 min at 600 °C, which was their optimum treatment.

a direct plasma CVD SiO_2 deposited on off-axis substrates for sputtered silicon interlayer thickness's of 10 and 20 Å, respectively. Both samples were annealed in N_2 at 600 °C for 30 min. The thickness of the interlayer is correlated with marked differences in the C–V characteristics. For the thinner silicon layer, as shown in Fig. 4(a), the hysteresis and the QS integral are similar to those presented in Fig. 2(a) where the silicon layer was deposited by MBE. For the thicker silicon layer, as shown in Fig. 4(b), we note a decrease in the hysteresis, an increase in the frequency dispersion and a decrease in the QS integral. From ellipsometry measurements after SiO_2 deposition, a silicon layer of the order of 4 Å was found for the sample with the thicker initial sputtered silicon layer.

The remote plasma enhanced CVD (RPECVD), as opposed to a direct plasma process, has been suggested as a less damaging process,[19] since the sample does not encounter the plasma directly. It has been used in conjunction with thin deposited silicon interlayers to obtain good C–V characteristics from MOS structures.[6,10] We have performed similar studies, where the interlayer of silicon has been deposited in the MBE system rather than in the RPECVD system. As shown in Fig. 5, we obtain C–V characteristics exhibiting low hysteresis and small frequency dependent shifts for n-type samples. Furthermore, our QS curves integrate to 0.6–

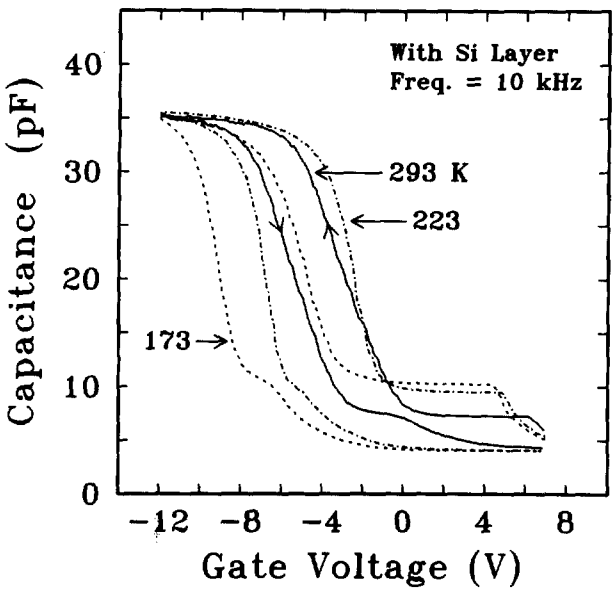

FIG. 3. 10 kHz C–V data for p-type GaAs oriented about 2° from the (100) axis. The sample has a silicon interlayer deposited *in situ* by MBE. The oxide was deposited by direct plasma enhanced chemical vapor deposition upon this air-exposed sample. The sample was then annealed in N_2 for 30 min at 600 °C. The results obtained at various temperatures (as labeled) are clearly varying. However, the increase from C_{min} to C_{max} is not delayed monotonically as the temperature is lowered; decreasing temperature from 293 to 223 K actually causes the increase in capacitance to occur at a lower gate bias.

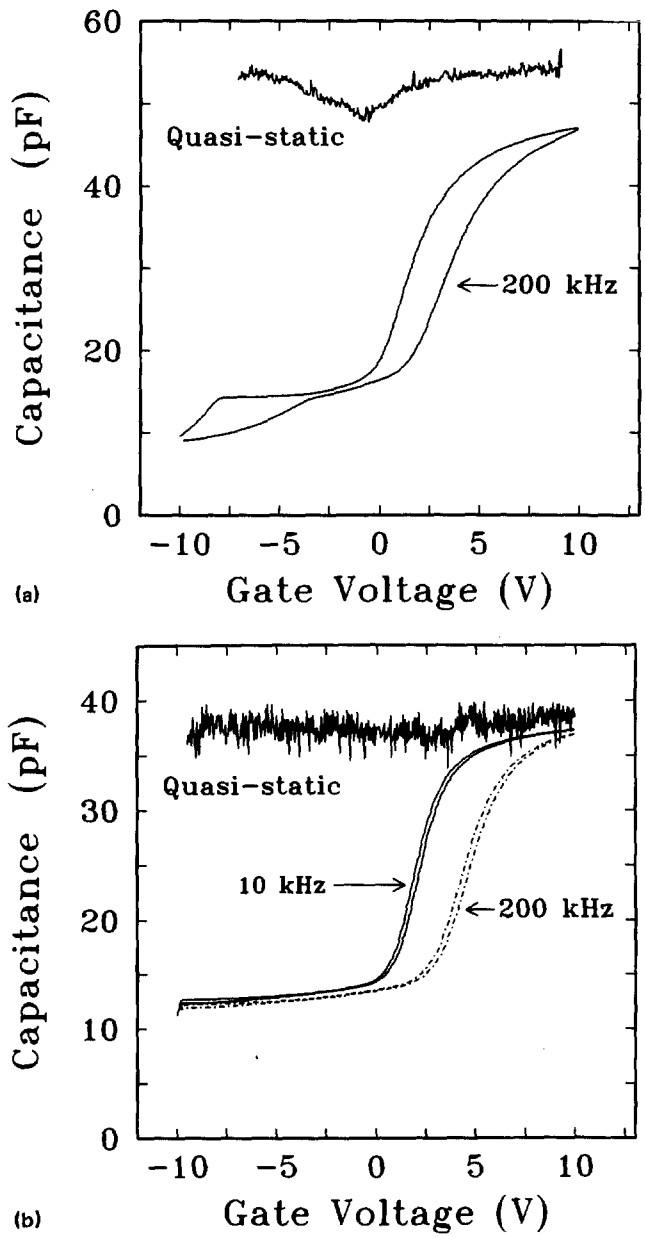

FIG. 4. 10, 200 kHz, and QS C–V data for n-type GaAs oriented about 2° from the (100) axis. The silicon interlayer was sputtered upon a bulk GaAs wafer following *in situ* cleaning. The oxide was deposited by direct plasma enhanced chemical vapor deposition *in situ* following the silicon deposition. For (a) the sample has about 10 Å silicon interlayer, while for (b) the sample has about 20 Å silicon interlayer. Both samples were annealed in N_2 for 30 min at 600 °C, which was their optimum treatment.

0.9 V, suggesting over half the band gap is accessible to the Fermi level under appropriate applied bias. These curves are superior to any we have obtained with other oxide deposition techniques tried so far. The same depositions and treatment without the interfacial silicon show a smaller QS integral, larger hysteresis, and a larger frequency shift. We should note, however, that the C–V curves from p-GaAs with the silicon interlayer do not show such good characteristics.

IV. DISCUSSION

The summary of electrical data contained in Table I suggests that the samples without a silicon interlayer with an on-axis substrate exhibits significantly better QS integrals, comparable hysteresis, and somewhat lower frequency dispersion than do the samples with the interlayer. The lower frequency dispersion can be related to the temperature dependence observed for a fixed frequency. In our description of Fig. 1 we inferred a minimum band bending of at least 0.45 V for the sample with a silicon interlayer and 0.33 V for the sample without a silicon interlayer. The sample with no silicon interlayer exhibits the smaller frequency dispersion which would be expected assuming a shift in the interface state distribution towards the conduction band edge. The better of these two samples did not have an interfacial silicon layer. These samples were purposely aligned more closely to the (100) axis than is normally the case, in an effort to reduce the density of steps and seek any impact of such a reduction. It has recently been suggested that a reduction in step density may lead directly to a reduction in interface state density and pinning behavior for well-ordered undamaged (100) GaAs interfaces.[8] We do in fact observe different behavior for these reduced step density samples, but cannot infer an improved interface state density. The behavior observed is not improved over the normally misaligned substrates, and we cannot rule out the possibility that the differences observed follow from the degraded morphology expected for on-axis substrates. In fact, the results for a sample with an off-axis substrate, MBE silicon interlayer, and a remote plasma SiO_2 film (followed by an optimized 600 °C

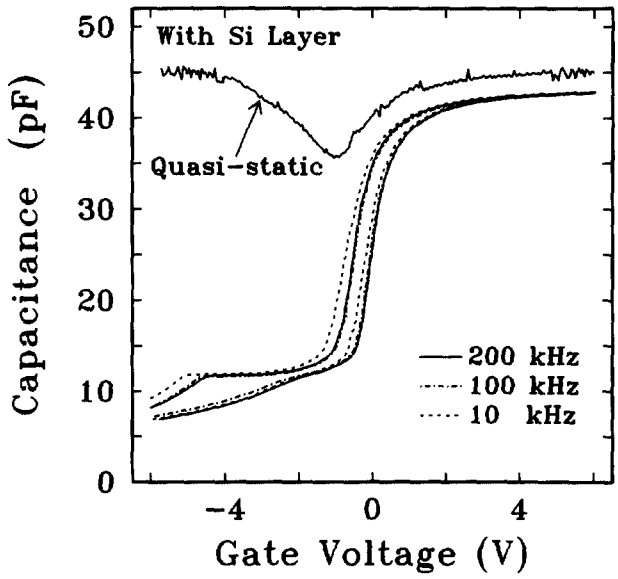

FIG. 5. 10, 100, 200 kHz, and QS *C–V* data for *n*-type GaAs oriented about 2° from the (100) axis. The silicon interlayer was deposited by MBE upon an MBE-grown layer. The oxide was deposited by remote plasma enhanced chemical vapor deposition upon this air-exposed sample. The sample was annealed in N_2 for 30 min at 600 °C.

anneal in N_2) were clearly superior to the best results obtained for the on-axis samples, as will be discussed next.

In Table II, results are summarized for *n*-GaAs (off-axis) samples with and without an MBE interlayer. The high temperature anneal clearly improves the QS integral where such could be obtained, generally reduces the hysteresis, but has a less well-defined effect upon the frequency dispersion. Further comparison between these two samples suggests that the QS integral is superior for samples with a silicon interlayer. The hysteresis and frequency dispersion are both apparently reduced (improved) for this sample. Comparison between the direct and remote PECVD oxides is more difficult. However, we can clearly note that the RPECVD oxide on the sample with a silicon overlayer clearly exhibits lower hysteresis and lower frequency dispersion, as well as a relatively large QS integral. This is true for the 600 °C annealed samples.

The differences between the samples with and without the MBE silicon interlayer are relatively small for the direct PECVD oxide. However, the optimum results clearly are for the RPECVD oxide on a sample with the silicon interlayer and these results are clearly superior both to those involving the same oxide on the no-silicon-interlayer sample and to the direct PECVD oxide on either *n*-type sample.

On the *p*-type samples (see Table II), the high-temperature anneal appears to improve the QS integral slightly, but it typically degrades the frequency dispersion, and for some samples increases the hysteresis. Furthermore, the impact of the silicon interlayer is less clear. For the direct PECVD oxide, the QS integral is larger for the sample without a silicon interlayer, but the hysteresis and frequency dispersion were improved by the presence of a silicon interlayer. For the RPECVD oxide, comparison QS integrals were typically not available (and slightly worse than the direct PECVD oxide when available), but frequency dispersion was degraded by the presence of the silicon interlayer.

To summarize, the high temperature anneal degrades the frequency dispersion for *p*-GaAs, but improves or has no effect on *n*-GaAs. The use of remote rather than direct PECVD reduces frequency dispersion for *n*-type GaAs with a silicon interlayer, whereas it degrades frequency dispersion for *p*-GaAs with a silicon interlayer. The high temperature anneal increases the QS integral, but there is a less convincing effect of the type of oxide deposition upon the QS integral.

We noted last year[9] that the frequency response relates to the separation of the interface pinning levels from the majority carrier band edge. In fact, as the pinning levels become further from the majority band edge, the frequency response at forward bias becomes degraded. We may well conclude, then, that the apparent improvement in *n*-type GaAs *C–V* curves induced by the use of RPECVD and a silicon interlayer has less to do with a reduction in overall interface state density than with a shift in position of those states to a region closer to the conduction band edge. This is consistent both with the concomitant degradation of the frequency dispersion of the *p*-type GaAs samples prepared in the same fashion, and with the less clear improvement in the QS integral associated with the use of a RPECVD rather than the direct PECVD. Some reduction in interface state density may also be inferred from our data. This is clearly consistent with the reduced pinning under the thin oxidized silicon interlayer studied by x-ray photoelectron spectroscopy (XPS)[9]—and with the inferred reduced damage to this film from the RPECVD oxide.

A shift in the interface state densities towards the conduction band edge suggests that this process is somewhat different from one attempting to achieve a silicon-like interface, where any region within the forbidden band gap is readily achieved under appropriate gate bias. The present situation may more closely resemble that of the MOS system in InP,[1] where relatively large interface state densities (on a silicon scale) did not preclude either good *n*-type *C–V* curves, nor *n*-channel inversion mode MOSFETs, since the pinning position at InP surfaces and interfaces permits the conduction band to be readily accessible. Of course, more recent results have also improved interface state densities for InP.[20] The normal situation for GaAs, where the Fermi level is pinned in the lower portion of the band gap, is less amenable to useful *n*-channel MOSFETs. The present results suggest a closer approach to the early InP situation; while not perfect, this is an improved situation for future GaAs-based MOSFETs.

ACKNOWLEDGMENTS

We gratefully acknowledge the technical assistance of J. Degelormo and R. Marks during various stages of this study. We are also grateful to J. Tsang for performing the Raman study of a sample and discussing the results with us.

[a] IBM, East Fishkill, Route 52, Hopewell Junction, New York 12533.

[1] L. G. Meiners and H. H. Wieder, Mater. Sci. Rep. 3, 139 (1988).

[2] E. Kohn and A. Colquhoun, Electron. Lett. **13**, 73 (1977).
[3] D. L. Lile, A. R. Clawson, and D. A. Collins, Appl. Phys. Lett. **29**, 207 (1976).
[4] S. Tiwari, S. L. Wright, and J. Batey, IEEE Electron. Dev. Lett. **9**, 488 (1988).
[5] B. Bayraktaroglu, E. Kohn, and H. L. Hartnagel, Electron. Lett. **12**, 53 (1976).
[6] G. G. Fountain, R. A. Rudder, S. V. Hattangady, R. J. Markunas, and J. A. Hutchby, Proceedings of the 1989 International Electron Devices Meeting (unpublished), pp. 89–887.
[7] R. E. Viturro, S. Chang, J. L. Shaw, C. Mailhiot, L. J. Brillson, A. Terrasi, Y. Hwu, G. Margaritondo, P. D. Kirchner, and J. M. Woodall, J. Vac. Sci. Technol. B **7**, 1007 (1989).
[8] J. L. Freeouf, J. M. Woodall, L. J. Brillson, and R. E. Viturro, Appl. Phys. Lett. **56**, 69 (1990).
[9] J. L. Freeouf, J. A. Silberman, S. L. Wright, Sandip Tiwari, and J. Batey, J. Vac. Sci. Technol. B **7**, 854 (1989).
[10] G. G. Fountain, S. V. Hattangady, D. J. Vitavage, R. A. Rudder, and R. J. Markums, Electron. Lett. **24**, 1134 (1988).
[11] Hideki Hasegawa, Masamichi Akazawa, Hirotatsu Ishii, and Kenichirou Matsuzaki, J. Vac. Sci. Technol. B **7**, 870 (1989).
[12] J. Batey and E. Tierney, J. Appl. Phys. **60**, 3136 (1986).
[13] B. Robinson, T. N. Nguyen, and M. Copel, AIP Conf. Proc. **167**, 112 (1988).
[14] J. L. Freeouf, Appl. Phys. Lett. **53**, 2426 (1988).
[15] J. L. Freeouf, Appl. Surf. Sci. **41/42**, 323 (1989).
[16] Dale M. Brown and Peter V. Gray, J. Electrochem. Soc. **115**, 760 (1968).
[17] T. Sawada and H. Hasegawa, Thin Solid Films **56**, 183 (1979).
[18] E. Kohn and H. L. Hartnagel, Solid State Electron. **21**, 409 (1978).
[19] G. Lucovsky, S. S. Kim, D. V. Tsu, G. G. Fountain, and R. J. Markunas, J. Vac. Sci. Technol. B **7**, 861 (1989).
[20] R. Iyer, R. R. Chang, and D. L. Lile, Appl. Phys. Lett. **53**, 134 (1988).