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Voltage-controlled photoetching of GaAs

H. J. Hoffmann,[a] J. M. Woodall, T. I. Chappell
IBM Thomas J. Watson Research Center, Yorktown Heights, New York, 10598

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The effects of optically generated minority-carrier current on the etching behavior of n-type GaAs in 1-M KOH aqueous solution were studied. It was observed that the etch rate depends on the minority-carrier current flow through the interface, which is controlled by the bias voltage. The etch rate is considerably reduced under open-circuit conditions as compared to short-circuit conditions. This effect simulates a self-limiting photoetching process for the thickness trimming of thin films, which is necessary for several device applications.

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The control and trimming of the thickness of thin GaAs layers plays an important role for device processing applications. The layer thickness can be reduced by well-known chemical or electrochemical etching procedures with or without illumination. (For a summary until 1978 see Refs. 1,2 and references cited therein). Until now, the purpose of most research in this field has been to improve the quality of the etched surfaces and to control and calibrate the rate of material removed.[3–13] For thin-film device applications, however, it is more important to control the thickness and uniformity of the remaining semiconducting layer. D. L. Rode, B. Schwartz, and J. V. DiLorenzo[5] and A. Shimano, H. Takagi, and G. Kano[11] describe a process how this can be achieved by anodic oxidation under illumination. In order to fabricate normally off field-effect transistors (FET's) by this process, however, one has to use rather high applied anodic bias voltages (up to 100 V) and one has to carefully control the light intensity. In contrast to this, we show in the present letter that the thickness of GaAs films can be controlled by a different self-limiting photoetching process with lower ($\leqslant 1$ V) or even without external anodic bias voltage.

For this investigation, we used chemomechanically prepolished (100) surfaces of n-GaAs samples with charge carrier concentrations in the range of $(1\text{–}5)\times 10^{17}$ cm^{-3}. The samples were prepared with sputtered Au-Ge alloy contacts on one side. The etching experiments were performed in a three-electrode electrochemical cell with a saturated calomel electrode (SCE) as the reference electrode, and a 4-cm^2 sheet of platinum as an auxiliary electrode. The GaAs samples were connected electrically with silver paste to metal electrodes inside a Teflon holder and subsequently cemented and partly covered with black wax. The sample area in contact with the electrolyte was varied from 4 to 25 mm.^{2} However, the photoetching current density was maintained constant using a large-area light source. All other parts of the working electrode were electrically insulated from the electrolyte by Teflon or black wax. The electrolyte was a 1-M aqueous KOH solution. The temperature was 26 ± 2 °C. The GaAs-electrolyte interface was either kept in the dark or illuminated uniformly through an interference filter with a transmission maximum at 550 nm and a full-width at half-maximum of 25 nm. The light intensity was 2.6 mW/cm^2.

Typical I-V characteristics without [curve (a)] and with [curve (b)] illumination of the GaAs-electrolyte interface are shown in Fig. 1. For zero current, there is a voltage between the sample and SCE of about (-0.6 ± 0.1) V in the dark and (-1.1 ± 0.1) V under illumination corresponding to an open-circuit photovoltage of about -0.5 V.

The etching experiments were performed using four different conditions. The first was etching in the dark without applying a bias voltage, and corresponds to point A in Fig. 1(a). For time intervals in the order of 2 or 3 h, aqueous KOH solution attack of the samples was not observed. This is in agreement with the fact that nearly all rapid chemical etchants for GaAs must have a strongly oxidizing component. (After keeping the samples in the KOH solution for 24 h, however, an etch groove of about 2-μm depth in the GaAs

[a]On leave of absence as a visiting scientist from Institut für Angewandte Physik, University of Karlsruhe, West Germany.

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along the boundary of the black-wax mask was seen.)

In the second case, the sample was etched under illumination at a potential corresponding to the potential at point A for zero current in the dark [point B in Fig. 1(b)]. In this case, nearly all of the minority carriers generated by the light in the depletion region reach the GaAs-electrolyte interface. There they contribute to the oxidation of the surface atoms which are subsequently dissolved in the electrolyte.[14-16] The flow of minority carriers toward the interface is proportional to the light intensity. An intensity of $2.6\ \mathrm{mW/cm^2}$ produced an etch rate of 2.1 Å/s (with an uncertainty of ± 0.3 Å/s probably due to the long-term instability of the lamp). This corresponds to an etching quantum efficiency of about 40% not correcting for reflection losses. The etch depth as a function of time is shown in curve (a) of Fig. 2. Even after etching times as long as 5 h, the surface quality was nearly as good as it was for the initial material.

For the third case, samples were etched under the same illumination as case 2 but with the GaAs-electrolyte contact forward biased to produce the same absolute value of the current as in point B [working point C in Fig. 1(b)]. Under these conditions, the samples were not etched even after several hours. This shows very clearly that the photoetching of GaAs is due to the net flow of minority carriers to the interface, since under forward bias, the flow of minority carriers to the interface is greatly reduced.

As a final step, the GaAs was etched under open-circuit conditions [working point D in Fig. 1(b)]. In this case, the etch rate is reduced by a factor of about 3 as compared to the etching at working point B. The etch depth as a function of time is shown by curve (b) of Fig. 2. The quality of the surface is also good. One can speculate about the mechanism responsible for the reduction of minority-carrier current flow through the interface. For the case of large densities of localized states at the interface, it is possible that at the open-circuit condition both the majority- and minority-carrier current would be equal at the interface, and hence carrier recombination at the interface would eliminate excess minority carriers flowing through the interface, which in turn would cause etching to stop. If this hypothesis were true, then the fact that the etching does not entirely stop could be explained by supposing that some of the majority current is drained off at regions in the sample other than in area of electrolyte contact. This would result in excess minority-carrier current passing through the interface which would cause etching. Alternatively, however, if the density of localized levels is small at the interface, then the reduction of minority-carrier flow across the interface would be related to the increase in carrier recombination within the GaAs which occurs at open-circuit or forward-bias conditions. The investigation of the dominant mechanism is currently being pursued.

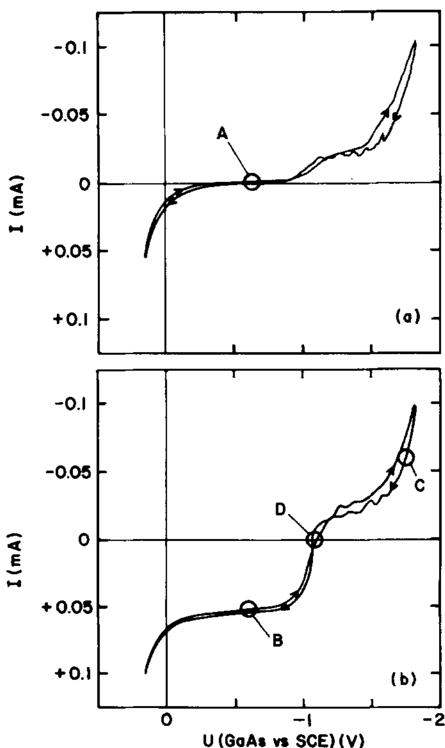

FIG. 1. I-V characteristics of the n-GaAs 1-M KOH solution cell in the dark (a) and under illumination (b). The sweep rate of voltage is 40 mV/s.

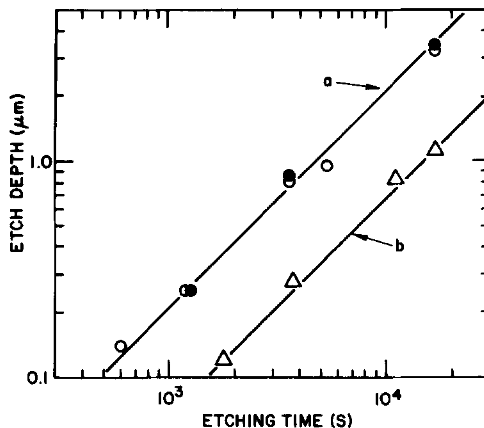

FIG. 2. Etch depth as a function of time for working point B [curve (a)] and D [curve (b)] of Fig. 1(b).

The results described in the present letter have important consequences for the semiconductor technology of thin n-type films on insulating and semi-insulating substrates. The etching experiments, especially at working points B and D, can be considered to simulate the trimming of the film thickness by photoetching. For this purpose, we consider a semiconductor film with thickness $d > l$ (l the depth of the depletion region at the semiconductor surface). As long as $d > l$, the film thickness can be reduced by photoetching under short-circuit conditions [working point B in Fig. 1(b)]. However, as $d \approx l$, the etch rate is slowed down considerably, since fewer minority carriers reach the semiconductor-electrolyte interface. This can be seen as follows: assume that the film thickness d is reduced further. Then the depth of the space-charge region on the surface must be reduced, too, since that region cannot be deeper than the film thickness itself. As a consequence of this, the band bending of the semiconductor-electrolyte interface will also be reduced and the layer becomes "pinched off" preventing the flow of majority carriers away from the illuminated area. Therefore, only a small fraction of the minority carriers generated by the illumination will flow through the semiconductor-electrolyte

interface, or in other words, the working point for the etching is shifted automatically from B towards D. The minority-carrier flow to that interface is reduced further because some of the minority carriers will flow to the back interface between the semiconducting film and substrate. Both effects lead to a self-limitation of the photoetching as d approaches the depletion layer thickness l.

In conclusion, a self-limiting thinning technique is desirable in order to control the film thickness over large areas. This is very important for device processing applications including solar cells and thin-film FET's; especially for the enhancement-mode thin-film FET for which one must control the film thickness to $d \approx l$. The present series of experiments have shown how the film thickness can be trimmed and controlled by photoetching. Using bias voltages which simulate open-circuit and short-circuit conditions, the etch rate can be varied a significant amount. These conditions occur automatically during the thinning of metal semiconductor field effect transistor structures and thus, photoetching is expected to be a useful self-limiting thinning technique for such structures.

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