n^+ InGaAs/nGaAs heterojunction Schottky diodes with low barriers controlled by band offset and doping level

A. W. Kleinsasser, J. M. Woodall, G. D. Pettit, T. N. Jackson, J. Y.-F. Tang, and P. D. Kirchner
IBM T. J. Watson Research Center, Yorktown Heights, New York 10598

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We have fabricated and measured low barrier (30–150 meV) Schottky diodes using n^+InGaAs/nGaAs pseudomorphic structures with up to 1.5% lattice mismatch. The I-V measurements at temperatures from 4 to 200 K show rectifying behavior and indicate transport mechanisms which range from tunneling to thermionic emission. The transport properties and barrier height determinations indicate that the band offset is predominantly in the conduction band. The barrier height increases with In concentration, which is consistent with band calculations based on previous experimental data.

I. INTRODUCTION

To first order the Fermi level is strongly but not precisely pinned at metal/III–V compound semiconductor interfaces.[1,2] Even though there are a variety of partially convincing models available to explain this behavior, these models do not as yet have the precision needed to aid in the development of suitable contacts to FET devices for LSI applications. In the case of GaAs, the major contact problems are a Schottky barrier for gate electrodes of about (but not exactly) 0.8 eV and an Ohmic contact metallurgy (i.e., Au–Ge–Ni) for source and drain electrodes which is unstable to subsequent processing above 400–500 C, whose contact resistance is highly dependent on subtle processing conditions and whose electronic interface properties are still not understood theoretically.[3] In spite of recent laboratory successes, it is quite possible that the variability in Schottky barriers and contact resistance using current technology could limit the usefulness of GaAs in LSI applications. In addition, it is not possible to arbitrarily change barrier heights and thus build devices which are optimized for low temperature applications where low barriers are needed.

It is well known that Fermi level pinning does not occur at carefully prepared lattice matched isoelectronic heterojunctions (e.g., GaAlAs/GaAs). Instead, the interface properties are determined by band alignment and doping. This fact has been successfully utilized in such devices as DH lasers and high electron mobility transistors. However, except for an early report by Chandra and Eastman[4] on GaAs/GaAlAs n–n heterojunctions, the band alignment properties have not been widely studied in structures which utilize majority carrier transport normal to the heterojunction (e.g., Schottky barrier diodes). Using advanced epitaxial growth techniques such as MBE and MOCVD, which permit good control of layer thickness, doping, and composition, it should be possible to fabricate these structures with barriers which meet device requirements.

In this paper we report first results on the I-V characteristics of low barrier (30–150 meV) Schottky diodes using n^+InGaAs-nGaAs heterojunctions, grown by MBE, in which the barrier height is controlled by band offset and doping level, rather than by Fermi level pinning.

II. TRANSPORT ACROSS SCHOTTKY BARRIERS

The flow of current in a metal–semiconductor (Schottky) contact is due to thermionic emission (TE) of electrons over, or tunneling of electrons through, the barrier. Tunneling, or field emission (FE), dominates at low temperatures (in which the electrons have insufficient energy to surmount the barrier) and in heavily doped material (in which the depletion width is small). In diodes having low barrier heights, the tunneling conductance at low temperatures can be substantial even for low donor concentrations. Due to the decrease in barrier width with increasing energy, the energy distribution of tunneling electrons can be rather narrowly peaked at an energy between the Fermi level and the top of the barrier at intermediate temperatures, giving rise to a well-characterized regime of temperature-assisted tunneling, or thermionic field emission (T-FE). A brief outline of the theory for conduction in these regimes will be useful in understanding our results, and is given here. The detailed form of the I-V characteristic has been a subject of much research; the interested reader is referred to the literature (see, for example, Refs. 2, 5, and 6 and references therein).

The current-voltage characteristic for transport over and/or through a barrier is Ohmic (linear) for low biases ($J = V/R_0$), and exponential for large biases ($J = J_s e^{qV/E_0}$). The parameters R_0, J_s, and E_0, and their dependence on temperature, contain information on the barrier, including the barrier height. In general, E_0 goes from a constant value characteristic of tunneling at low temperatures to kT (or some multiple of kT) at high temperatures, due to thermionic emission (deviations from kT may be due to image force lowering of the- barrier, contributions to the current due to tunneling, or other effects.[2,5,6] For a Schottky barrier,

$$E_0 = E_{00}\coth(E_{00}/kT), \tag{1}$$

where

$$E_{00} = (qh/4\pi)(N_D/\epsilon m^*)^{1/2} \tag{2}$$

is a characteristic energy for tunneling.[2,5,6] The three regimes of conduction are defined by $E_{00} \gg kT$ for FE, $E_{00} \sim kT$ for T-FE, and $E_{00} \ll kT$ for TE. The product $J_s R_0$ is another characteristic voltage, ranging in value from $\simeq E_{00}$ in the FE regime, to kT in the T-FE and TE regimes. The major barrier

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height (E_B) dependence is contained in R_0 (or J_s) with $R_0 \propto e^{E_B/E_0}$. The theoretical behavior of J_s, R_0, and E_0 will be illustrated below along with our results.

III. THEORY OF BAND OFFSET DIODES

In a contact between two dissimilar semiconductors (a heterojunction) there is an interfacial discontinuity of the conduction and valence bands due to the difference in energy gaps. The band lineup at heterojunction interfaces is not well understood,[7–9] however this lineup determines the magnitude of the discontinuities, and the resulting barriers govern carrier transport across the interface.

When two similarly doped semiconductors are combined to form an isotype heterojunction, the discontinuous change in band structure at the interface gives rise to band bending in the conduction and valence bands.[10] (In some cases Fermi level pinning, due to interfacial impurities or misfit dislocations[11] can determine the band bending. This is not the case in our abrupt lattice-matched heterostructures.) In many cases, such as InGaAs/GaAs, most of the band gap discontinuity is taken up by the conduction band,[9] giving the possibility of majority carrier devices based on controllable barriers to electron transport. The band bending in heavily doped n^+InGaAs is minimal, and the upward bending of the conduction band in low-doped nGaAs results in a Schottky barrier diode, in which the InGaAs plays the role of the metal contacting an n-type semiconductor.

In order to model the conduction band bending, Poisson's equation for the InGaAs/GaAs heterojunction system was solved by MONTE, a general device simulator[12] which incorporates Fermi-Dirac statistics for the electron gas and uses a finite difference scheme. In equilibrium, Poisson's equation is highly nonlinear in potential, because of the right hand side, and has to be solved by Newton's method. Band offsets, density-of-states effective masses and temperature can be adjusted as inputs to the program. In our case, it was assumed that the conduction band discontinuity was 85% of the band gap difference,[7,9] which is a known function of composition.[13] The conduction band discontinuity and band bending for the case of $In_{0.15}Ga_{0.85}As$ with doping levels of $1\times10^{18}/2\times10^{16}$ cm^{-3} (InGaAs/GaAs) are illustrated in Fig. 1.

The barrier height, E_B, for the heterojunction is approximated by $E_B \simeq \Delta E_c - \xi_2$, where ΔE_c is the total conduction band offset at the interface and ξ_2 is the Fermi level degeneracy in the InGaAs layer (the exact result includes the small band bending in the InGaAs and ξ_1, the Fermi level degeneracy in the GaAs.) Thus, the diode barrier height is determined primarily by the In fraction (ΔE_c) and the n doping (ξ_2) in the InGaAs layer. This barrier height is adjustable over a wide range by fabrication parameters.

The bending of the GaAs conduction band is well described by the standard equations for metal–semiconductor Schottky barriers[2]:

$$E(x) = (E_B - qV + \xi_1)(1 - x/w)^2 - \xi_1, \tag{3}$$

with energy measured from the semiconductor Fermi level (see Fig. 1); the depletion width is

$$w = [(2\epsilon_s/N_D q^2)(E_B - qV + \xi)]^{1/2}. \tag{4}$$

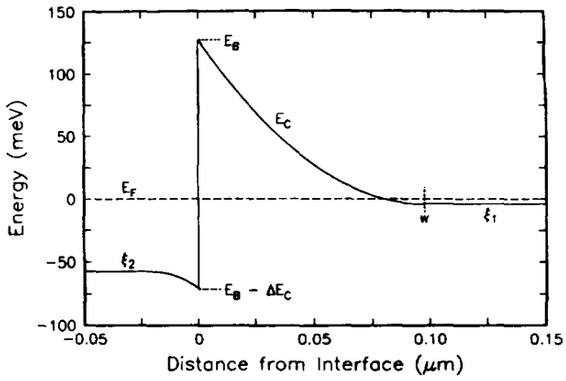

FIG. 1. Band bending of the conduction band at the $n^+In_xGa_{1-x}As/n$-GaAs heterojunction interface in absence of applied bias. In this example, $x = 0.15$, $\Delta E_c = 198$ meV, $E_B = 125$ meV, $\xi_1 = 4$ meV ($N_D = 2\times10^{16}$), $\xi_2 = 60$ meV ($N_D = 1\times10^{18}$), and $w = 96$ nm.

In our calculations of I-V characteristics, these relationships were used along with barrier height and Fermi level positions obtained from the simulation described above. It was assumed that $N_D^+ = N_D$ at all temperatures for the dopant concentrations used in these experiments.

IV. EXPERIMENTAL PROCEDURE

The structures used in this study were prepared by the MBE method. A cross section showing doping and layer sequence is shown in Fig. 2. It should be noted that great care was taken to make sure that the InGaAs layer was thin enough to be pseudomorphic (i.e., no misfit dislocations were formed at the InGaAs/GaAs interface). This is the major reason why the top n^+ layer was graded back to GaAs. Early attempts to grade the top n^+ layer to pure InAs to aid in Ohmic contact formation resulted in misfit dislocation formation at the critical InGaAs/GaAs interface. Previously, it was shown[11] that misfit dislocations are electrically active and will pin the Fermi level and thus introduce spurious effects when trying to determine the effects of band off-

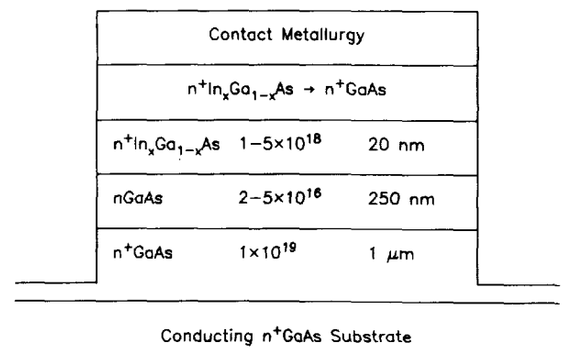

FIG. 2. Schematic of cross section of the experimental structure described in the text. The heterojunction occurs at the interface between the nGaAs and the n^+InGaAs. The composition of the InGaAs layer above the first 20 nm is graded to pure GaAs. Au–Ge–Ni contacts are made to this layer and to the substrate.

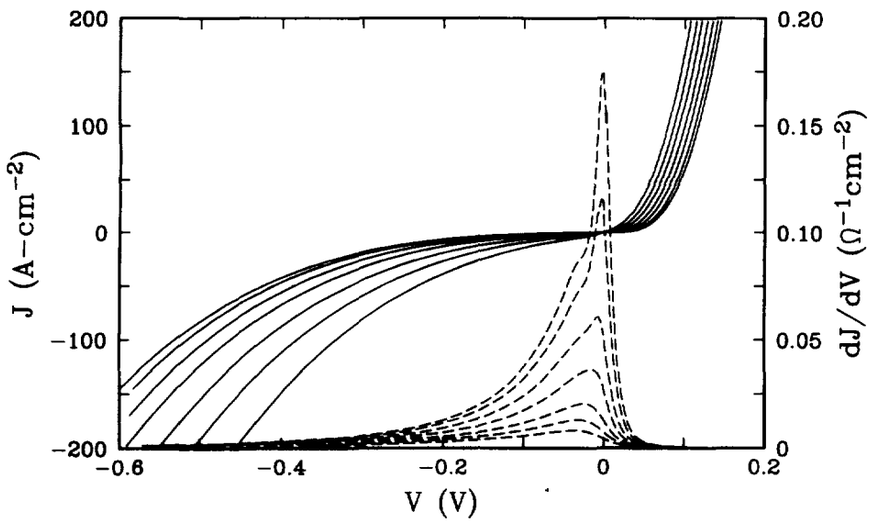

FIG. 3. Current (solid curves) and dynamic resistance (dashed curves) vs voltage for a $n^+In_{0.20}Ga_{0.80}As/nGaAs(5\times10^{18}/2\times10^{16})$ heterojunction at various temperatures (4.2, 23, 40, 55, 70, 85, 101 K).

set. Also, great effort was made to achieve low resistance Au–Ge–Ni Ohmic contacts to the structures to assure that the contact resistance was lower than the junction resistance, and that the alloying did not penetrate to the active region of the junctions. The junction area was defined by mesa etching in which the etching was terminated above the epi/substrate interface. This was done to eliminate possible deleterious effects, such as Fermi level pinning at that interface, on the *I-V* characteristics of the band offset junction.

The junctions were studied through current-voltage characteristics, which were measured at temperatures ranging from 4.2 to $\simeq$200 K (Junction conductance was too large at higher temperatures, even with the largest barrier heights studied, and conductances were limited by other parts of structure.). Sample temperature was varied by varying the height of a cryoinsert containing the chip above a hellum bath. Temperature was stabilized during data acquisition using a feedback-controlled resistance heater (the temperature measurement and control was good enough that no differences were observed in the characteristics between immersion of the sample in liquid nitrogen and cooling to 77 K in helium vapor). The *I-V* data were obtained using a microcomputer-controlled current source and voltmeter. Dynamic resistance was obtained digitally from the *I-V* points.

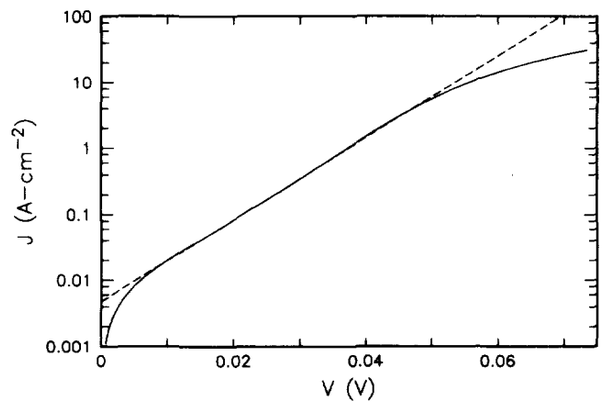

FIG. 4. Semilog (forward) current-voltage characteristic for a $n^+In_{0.15}Ga_{0.85}As/nGaAs$ ($1\times10^{18}/2\times10^{16}$) heterojunction at 4.2 K.

V. RESULTS AND DISCUSSION

The current density J and dynamic specific resistance (dV/dJ) of a typical diode are plotted as a function of voltage in Fig. 3, at temperatures ranging from 4.2 to 100 K. Rectification, a strong increase in current with temperature, and a resistance maximum at negative bias, all predicted by theory[6,14] for these structures, are illustrated.

Figure 4 is a semilog plot of forward current density vs voltage for another sample at 4.2 K, illustrating the exponential *I-V* characteristic in the tunneling regime. The decrease in slope at $\simeq$45 mV is due to series resistance,[5] which will be discussed below. In this sample, $N_D = 1\times10^{18}$ (2×10^{16}) cm^{-3} in the $In_{0.15}Ga_{0.85}As$ (GaAs) layer. Fitting the curve using $J = J_s e^{qV/E_{00}}$ gave values of 0.0048 A cm^{-2} for J_s and 6.99 meV for E_{00}, indicating $N_D = 1.24\times10^{17}$ cm^{-3} [see Eq. (4)]. This sort of discrepancy between sample doping and the N_D value extracted from E_{00} was observed in all samples. Inclusion of image force lowering in the barrier shape (not included in the theory of Ref. 6) would help to explain the larger than expected values of E_{00}.[15] The product of J_s and R_0 was 3.5 meV, approximately what is expected from the theory of tunneling in Schottky barriers.[6] For the best fit of the *I-V* to theory,[6] we obtain a barrier height of 127 meV, compared with 125 meV obtained from our band structure simulations. This apparently excellent agreement should be taken only as an indication that the true barrier height is in this range. Even if the ideal barrier shape (without image force lowering) assumed in the theory is correct, the carrier concentrations, Fermi level positions, and the conduction band offset at the interface were not determined experimentally ($\Delta E_c = 0.85\Delta E_G$ was assumed here). Also, image force lowering is expected to reduce the peak barrier height by

$$\Delta\phi \simeq E_B \pi^{-1/2}(E_B/E_{11})^{-3/4}, \tag{5}$$

where $E_{11} = (q^2/2)(N_D/\epsilon_s\epsilon_d^2)^{1/3}$, with ϵ_s and ϵ_d the static and

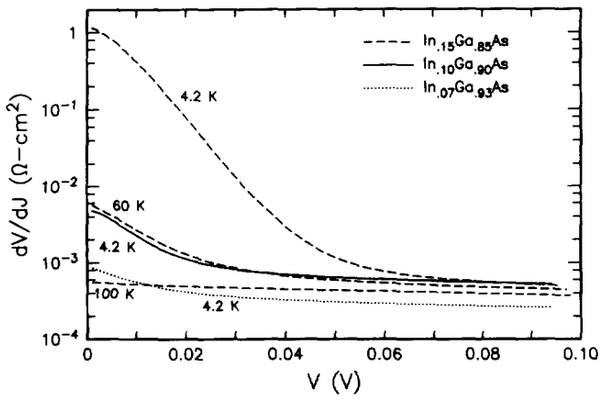

FIG. 5. Semilog plot of zero-bias dynamic resistance (dV/dJ) vs V for the diode of Fig. 4 at 4.2, 60, and 100 K, along with 4.2 K characteristics for $In_{0.10}Ga_{0.90}As$/GaAs and $In_{0.07}Ga_{0.93}As$/GaAs devices. Barrier heights estimated from simulations were 125, 67, and 31 meV.

dynamic dielectric constants of the semiconductor.[15] This lowering is significant for the low barriers of interest here.

Figure 5 is a plot of dV/dJ vs V for the same sample at three temperatures (4.20, 60, 100 K), along with 4.2 K data for two samples which were identical to it in doping and layer thickness (to within the limits of control for the deposition system), but which differed in In content ($In_{0.07}Ga_{0.93}As$ and $In_{0.10}Ga_{0.90}As$, vs $In_{0.15}Ga_{0.85}As$ in the earlier sample). The figure illustrates the dramatic increase of conductance with temperature and the increase in conductance with decreasing barrier height. These will be discussed below.

Also illustrated in the figure is the problem of series resistance. For large biases, in excess of the barrier height for the heterojunctions, most of the voltage drop is across a series resistance which consists of a constant resistance and an exponential resistance; the latter term is presumably related to the contacts to the GaAs top and bottom layers in the structure. The series resistance varied little among the samples shown, and was not very temperature dependent. These samples were extreme in that the series resistance was large due to accidental low doping in the top and bottom GaAs films. Other samples were qualitatively similar, but approximately equal to two orders of magnitude more conductive at large voltages. The series resistance limits meaningful measurements to low voltages. Comparison of JR_0 vs V for the three samples of Fig. 5 provided an indication of the maximum useful voltage (at 4.2 K) for each. The scaled current-voltage characteristics were almost identical among these samples at low voltages. Deviations due to the series resistance occurred at progressively higher voltages for higher In concentrations (higher barrier heights). This is evidence that the low voltage behavior was due to the interface and not some other part of the structure. It is clear that the series resistance became dominant even at low voltages for $T > 100$ K in the $In_{0.15}Ga_{0.85}As$ sample, and may have contributed, even at low bias, to the conductance of the $In_{0.07}Ga_{0.93}As$ sample, even at 4.2 K. This contact resistance is not a fundamental problem at present; values approaching $10^{-7}\ \Omega\ cm^2$ at zero bias should be possible. However, the use of very low barriers in cryogenic devices may require even lower series resistances, in which case a new contact process would be required.[16]

The temperature dependence of the I-V parameters is a useful confirmation that the structures behave as Schottky barrier diodes, in general accordance with theory. Figure 6 illustrates this for the sample of Fig. 3. The solid circles represent $R_0 \equiv |dV/dJ_{v=0}$ vs temperature. The data are well fitted by the solid curve, obtained using the 4.2 K values of R_0 and $E_{00}\ \xi_1 = 9$ mV, and the theory of Ref. 6. The barrier height was a fitting parameter; in this case E_B was 120 meV. The FE and T-FE regimes are defined on the graph by vertical lines (the analytic expressions of Ref. 6 are not valid in the intermediate region). The $J_s R_0$ product (open circles) is essentially constant for FE and equals kT in the T-FE and TE regimes. The dashed lines represent the theory, which is followed reasonably well using the same parameters. The value of E_0 (solid triangles) rises much more rapidly than expected (theory is the dotted curve) in the T-FE region, and appears to approach the dotted line $E_0 = nkT$ (with $n \simeq 1.6$, independent of temperature) as T approaches $\simeq 100$ K (the value 1.6

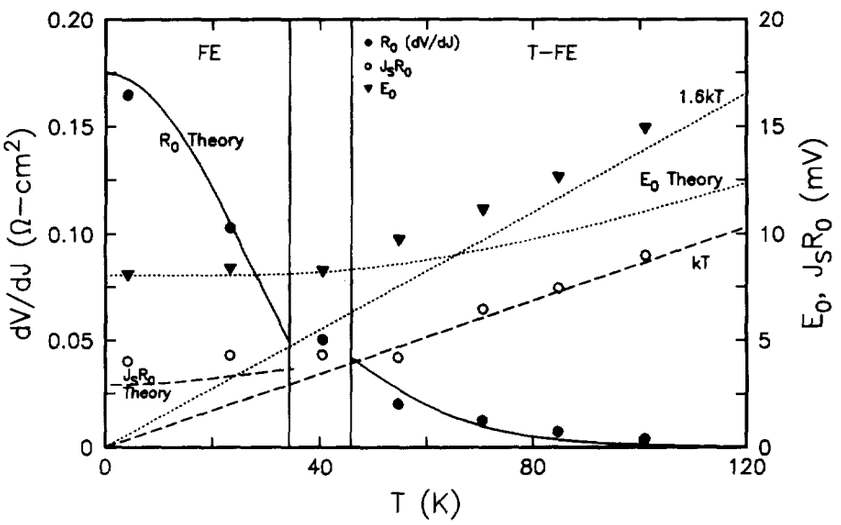

FIG. 6. Current-voltage parameters (J_s, R_0, and E_0) as a function of temperature for the device of Fig. 3, along with theoretical fits (see text).

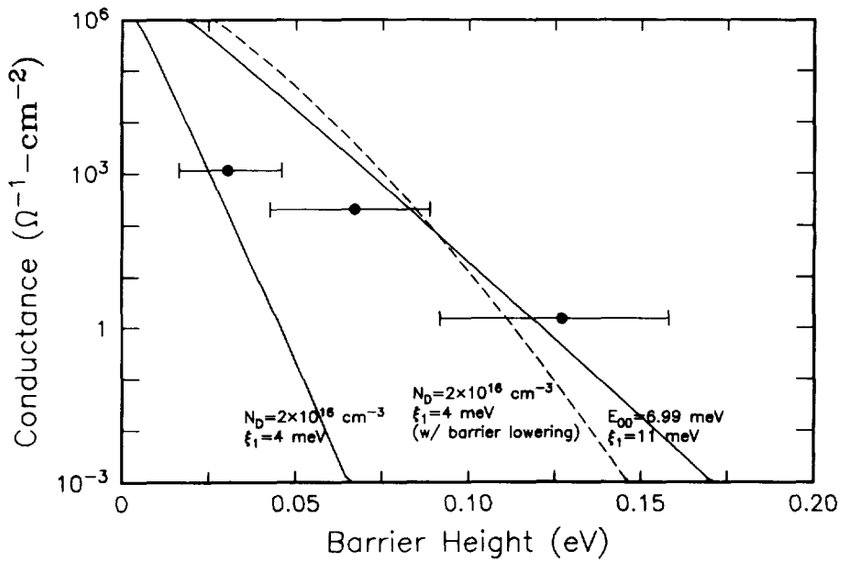

FIG. 7. Zero-bias conductance vs barrier height for $In_xGa_{1-x}As$ ($x = 0.15$, 0.10, and 0.07) structures of Fig. 4, along with various theoretical dependencies discussed in the text. Barrier heights for the experimental points were obtained from simulations, assuming that the conduction band discontinuity was 85% of the band gap difference. The "error bars" show the shift of the points if 70% and 100% are used.

was obtained from data for several samples for temperatures as high as 180 K). The $e^{qV/nk}$ behavior of the current in the T-FE regime is consistent with the addition of a thermionic emission component to the current.[5] It is doubtful that such a component would be of significance at these temperatures unless the barrier shape deviated from that of Eq. (3). Image force lowering of the barrier would account for the increase in the TE component in the T-FE regime.[15]

Figure 7 is a plot of zero bias conductance (4.2 K) vs barrier height for the family of samples of Fig. 5. Barrier heights were obtained from the simulations described earlier; E_B values were 125, 67, and 31 meV for $In_xGa_{1-x}As$, with $x = 0.15$, 0.10, and 0.07. The two solid lines in the figure are from the theory of tunneling in Schottky barriers[6] for the GaAs doping (2×10^{16}) and for the doping implied by $E_{00} = 6.99$ meV (1.24×10^{17}). The data fall somewhere in between. Image force lowering of the barrier causes an increase in the tunneling exponent to a value $E_t > E_{00}$.[15] Using the value of E_t obtained by evaluating the WKB transmission probability integral with $N_D = 2\times10^{16}$, the barrier lowering of Eq. (5) and the tunneling expressions of Ref. 6, the dashed curve was obtained (the barrier height plotted is the value without lowering, because this is the number obtained in our simulations). Althouth the data are not well fit by the new curve, barrier lowering may be important in explaining the large values of E_{00} encountered in all of our samples, as well as the temperature dependence of E_0. Samples with E_B in excess of roughly 100 meV had conductances which agreed reasonably well with predictions (see either the dashed curve or the $E_{00} = 6.99$ meV curve). This agreement includes other samples with different parameters not included in the figure. For lower barrier heights, the increase in conductance with decreasing barrier height was slower than expected.

The horizontal error bars of Fig. 7 were obtained from simulations assuming that 70% and 100% of the energy gap difference is taken up in the conduction band, rather than 85%. These "error bars" are rather extreme, however, the subject of band lineup is still controversial, and our experimental points would be shifted to the right or left if the 85% number were not correct. Note that, at least for barrier heights in excess of $\simeq$100 meV, the agreement between the barrier heights obtained from band structure simulations and from tunneling theory indicate that the 85% is close to the correct figure.

The conductances for the low barrier height samples were evidently lower than expected. In addition to the assumptions described earlier, several possibly important effects, such as traps in the semiconductor, space charge limited current flow,[5] and the fact that the "metal" in these Schottky barriers is actually a degenerate semiconductor, were not considered in the theory. Another important consideration is the reduction of the depletion width to lengths approaching the inter-donor spacing. Although this effect is usually of concern in heavily doped samples,[5] because $w/N_D^{-1/3} \propto N_D^{-1/6}$, it is also important in low barrier samples even at modest doping levels. For a 50 meV barrier, the depletion width in 2×10^{16} GaAs, even at zero bias, is only approximately equal to 2 inter-donor spacings. Such effects may be expected to play a significant role in the barrier height dependence of device conduction. Further experiments are clearly indicated if such effects are to be explored. It will be important to obtain direct information on carrier concentrations, Fermi level positions, and conduction band offset. In any case, it is clear that we have been able to produce barriers of small and controllable height.

VI. CONCLUSIONS

We have produced low (30 to 150 meV) barrier n^+InGaAs/nGaAs heterojunction Schottky diodes, in which the barrier height is continuously adjustable, primarily through two fabrication parameters, the donor concentration in the n^+ layer, and the composition of the ternary layer. Conduction at small biases in diodes with barrier heights in excess of $\simeq$100 meV could be accounted for by the theory of tunneling and temperature-assisted tunneling in Schottky diodes. At larger biases, in the exponential region of the I-V characteristic, the magnitude and temperature dependence of the ex-

ponent were both larger than expected, probably due to the role of image force lowering of the barrier.

For lower barrier heights (below $\simeq$ 100 meV), the behavior of the diodes was qualitatively similar to those with larger barriers. However, the increase in diode conductance with decreasing barrier height, although exponential, was somewhat slower than expected. Several physical effects, including space charge limited current and the breakdown of the continuum model for the semiconductor depletion region as the depletion width approaches the average inter-donor spacing, have not been taken into account, and illuminate the possibility of new and interesting physics in the new regime of millivolt barriers.

We have demonstrated for the first time Schottky barrier diodes with continuously adjustable barrier heights (down to the millivolt range) and depletion widths. These devices offer an alternative to metal–semiconductor Schottky barriers, in which the barrier height is determined by Fermi level pinning.

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