n-InAs/GaAs heterostructure superconducting weak links with Nb electrodes

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We report on the fabrication and characterization of planar superconductor-normal-superconductor (SNS) weak links in which the normal region is deposited *n*-InAs. The InAs is part of a heterostructure consisting of 100 nm of *n*-InAs grown on an undoped GaAs buffer layer on a semi-insulating GaAs substrate. The superconductor is Nb, patterned by electron beam lithography with interelectrode spacings as small as 260 nm. Device behavior is well explained by SNS weak link theory, with coherence lengths calculated from measured material parameters. These heterostructure weak links can be the basis for superconducting field-effect devices. They have the significant advantage of allowing simple device isolation compared with bulk InAs, which has been used in previous attempts to make such devices.

Recognition of the need for three-terminal devices for cryogenic circuit applications has resulted in renewed interest in superconducting field-effect transistors (FET's),[1–4] which were first proposed a number of years ago.[5–7] These are superconductor-normal-superconductor (SNS) weak links in which the link is a semiconductor, allowing the strength of the Josephson coupling (i.e., the supercurrent) to be controlled by adjusting the carrier concentration in the link (or FET channel) via a gate.

The original superconducting FET proposals[5–7] emphasized the use of materials such as InAs for the channel because, in these materials, the pinning of the Fermi level in the conduction band at surfaces and interfaces results in Schottky barrier-free contacts; the presence of such barriers in a superconducting FET device would decrease the maximum available supercurrent, reduce the degree of control of the supercurrent via the gate, and represent a significant series resistance in the device. Both Si[1,2] and InAs[3,4] have been used in the recent superconducting FET experiments. The absence of Schottky barriers, low effective mass, and high carrier mobility in InAs allow significantly larger device lengths and/or lower dopings for InAs compared with Si (for a given Josephson critical current). However, the InAs devices have two major drawbacks, namely, very poor response to applied gate bias and lack of device isolation. The application of several volts to the gate of a Nb/*p*-InAs/Nb device changes the critical current or device resistance by considerably less than a factor of 2,[3,4] due to strong pinning of the surface Fermi level at the channel-gate insulator interface. As for device isolation, the use of *p*-InAs allows vertical isolation, since a surface inversion layer is separated from the conductive substrate by a depletion region, but the presence of a conducting layer over the entire surface of both *n*- and *p*-type InAs crystals, even after etching of mesas, results in low values for the critical current-resistance ($I_C R_N$) product (which is an important figure of merit for Josephson weak links)[3,4,8] and makes it difficult to laterally isolate devices.

The semiconductor-coupled SNS weak link structure which forms the basis for these superconducting FET's is of interest in its own right for some potential applications of Josephson devices. Weak links, particularly SNS junctions, are attractive primarily due to their low capacitance. In order to achieve reasonable resistances and large $I_C R_N$ products, many workers have advocated using semiconductors as a link material.[9,10] Semiconductor-coupled weak links have been made, primarily on Si[2,10,11]; however, the behavior of these devices is not well understood; in particular the $I_C R_N$ values are considerably larger than expected,[11,12] possibly due to a SINIS structure (S and N are the superconductor and normal semiconductor layers and I is the insulating depletion region due to the Schottky barrier at the metal-semiconductor interface). InAs-coupled links have been made[8]; however, they suffer from low $I_C R_N$ values.

In this letter, we describe the use of an *n*-InAs/GaAs heterostructure to produce Nb/InAs/Nb weak links with high $I_C R_N$ products and excellent isolation. In addition to their potential as high quality Josephson devices, these links can form the basis for improved Josephson FET devices. This scheme also introduces the possibility of modulation-doped superconducting FET's and similar device structures.

The heterostructures consisted of 100 nm of *n*-InAs, grown on undoped GaAs buffer layers on semi-insulating GaAs substrates by molecular beam epitaxy and schematically illustrated in the inset to Fig. 1. Although there is a large ($\simeq 7\%$) lattice mismatch between GaAs and InAs, excellent layers were obtained. The films were mirrorlike with only occasional small surface defects. It was possible to dope the layers *n* type with Si over several orders of magnitude of dopant concentration. Room-temperature Hall-effect electron mobilities were 5000, 2000, and 1900 $cm^2/V\,s$ for dopings of 3.5×10^{17}, 3.5×10^{18}, and 3.1×10^{19} cm^{-3}, with no significant change on cooling to liquid-nitrogen temperature. For comparison, in the weak link experiment on bulk *n*-InAs,[8] mobilities of 16 900 and 10 000 $cm^2/V\,s$ for dopings of 2.5×10^{17} and 2.6×10^{18} cm^{-3} were reported. The mobilities in the lightly doped layers were below those expected for bulk InAs, possibly due to defects resulting from the large lattice mismatch; however, growths on lattice-matched substrates (e.g. *p*-InAs) for comparison have

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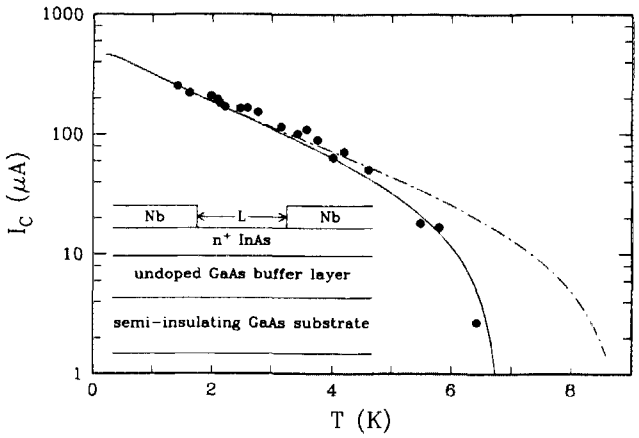

FIG. 1. Temperature dependence of critical current for a weak link on 3.5×10^{17} cm^{-3} n-InAs. The low-temperature dependence, dominated by the $T^{-1/2}$ dependence of ξ_N, is sensitive to the value of $L/\xi_N(T_C)$. A value of 60 nm is obtained for ξ_N at 4.2 K. The curves are fitted to the data using Eq. (2) with an adjustable prefactor. T_C values of 8.84 and 6.8 K were assumed for the dashed and solid curves, respectively. The inset is a schematic diagram of the device structure. The InAs and Nb layers are 100 and 60 nm thick, respectively, and link length L is as small as 260 nm.

not been done. In the layers with the heaviest doping, electron mobilities were closer to those expected for bulk InAs at that doping.

The use of thin InAs allowed both vertical and lateral isolation of the devices, since device mesas could be formed by etching through the InAs layer to the insulating substrate. Also, channel thickness could be controlled by the InAs film thickness, and is not limited to a thin surface inversion layer.

Device processing involved three masking levels. First, the device mesas were patterned using optical lithography and etched with an Ar ion beam. Next a lift-off stencil for the Nb superconducting electrodes was defined in a double layer resist by electron beam lithography. Gaps between the Nb electrodes (device lengths) ranged from 0.26 to 3 μm. The device widths ranged from 25 to 200 μm. The Nb electrodes, 50–65 nm thick, were deposited by electron beam evaporation. T_C was 8.8–9 K; essentially the same value was obtained in InAs as on accompanying oxidized Si substrates. An rf sputter preclean of the InAs (2.6 Pa Ar, $-200V_{dc}$, 3 min) was used prior to Nb deposition by electron beam evaporation. Au/Cr wiring, patterned by optical lithography, was used to connect devices to bonding pads on a periphery of the chip.

The 3.5×10^{17} sample was processed to completion. Current-voltage (I-V) measurements were made at 4.2 K on 21 devices. Device lengths were measured in a scanning electron microscope after the electrical measurements. The gaps between the Nb pads defining the weak links were uniform, with an estimated roughness of approximately 0.03 μm. The measured resistivities were in reasonable agreement with the Hall-effect results down to the smallest gaps, indicating that the contact resistance was quite low. Supercurrents were observed at 4.2 K in the four shortest devices. Any supercurrents in the longer links were below $\simeq 1\,\mu$A. The I-V characteristics exhibited the excess current characteristic of SNS weak links. The I-V curves were nonhysteretic, except that the I-V for the smallest sample (0.26 μm) became hysteretic at temperatures below 3 K.

The critical current of a semiconductor-coupled SNS weak link varies with device length L as $\exp(-L/\xi_N)$, where

$$\xi_N = (\hbar^3\mu/6\pi mek_BT)^{1/2}(3\pi^2 n)^{1/3} \quad (1)$$

is the normal metal coherence length (μ,m, and n are the electron mobility, effective mass, and density in the semiconductor).[10] The I_CR_N product for SNS weak links was obtained by Likharev.[13] For long links ($L\gg\xi_N$) not too far from T_C,

$$I_CR_N = [4\Delta^2(T)L/\pi ek_BT\xi_N]e^{-L/\xi_N}, \quad (2)$$

where I_C is the maximum Josephson supercurrent and R_N is the normal state resistance.

At low temperatures, the temperature dependence of the critical current is dominated by the $T^{-1/2}$ variation of ξ_N, and is therefore very sensitive to L/ξ_N, providing a good method for determining ξ_N (fits to the data become very poor if the L/ξ_N ratio deviates by more than $\simeq 10\%$ from the value used for an optimum fit). Figure 1 is a plot of the temperature dependence of critical current for the shortest link ($L = 0.26\,\mu$m). Fitting the low-temperature data (below $\simeq 4$ K) to the temperature dependence implied by Eq. (2) gives a value of 4.35 for L/ξ_N at 4.2 K, implying a value of 0.060 μm at 4.2 K. To obtain the value $\xi_N(4.2\text{ K}) = 0.060$ μm from Eq. (1), using the measured values of mobility and carrier density for this wafer, requires an effective mass of 0.048 for the InAs. The textbook value[14] is 0.023; however, at 3.5×10^{17} cm^{-3} the Fermi level is well into the conduction band, and the effective mass is larger than the value at the band minimum,[15] and the value 0.048 is not unreasonable. The dashed line in Fig. 1 is a fit to the data using the temperature dependence of Eqs. (1) and (2), using $L/\xi_N(4.2\text{ K}) = 4.35$ and a prefactor chosen to fit the data at 1.4 K. The data drop significantly below the theory curve above $\simeq 4$ K. This sort of deviation is common in SNS junctions, and may be related to the proximity effect on the superconductor.[9] The solid line in the figure was obtained in the same way, but using $T_C = 6.8$ K, the temperature at which the observed critical current disappears; this lower T_C presumably represents the transition temperature of the SN bilayer. Note, however, that the electrode T_C is 8.84 K; at this temperature the I-V characteristic changes resistance dramatically as large areas of Nb go normal. Thus, the meaning of the lower T_C is not completely clear.

Figure 2 is a plot of critical current (divided by electrode width) as a function of device length. The solid circles are our data, while the open circles were obtained from Ref. 8 from links on bulk n-InAs with essentially the same doping (the data given in that paper were for 2 K; the 4.2 K values were obtained from the known temperature dependence). There appears to be some consistency between the two experiments. Unfortunately, although all of the data in the figure are for essentially the same doping, the coherence lengths for the bulk sample and our thin InAs sample are different, due to the differing mobilities. The two lines in the figure are included to show consistency with the expected $\exp(-L/\xi_N)$ dependence (the lines are drawn arbitrarily

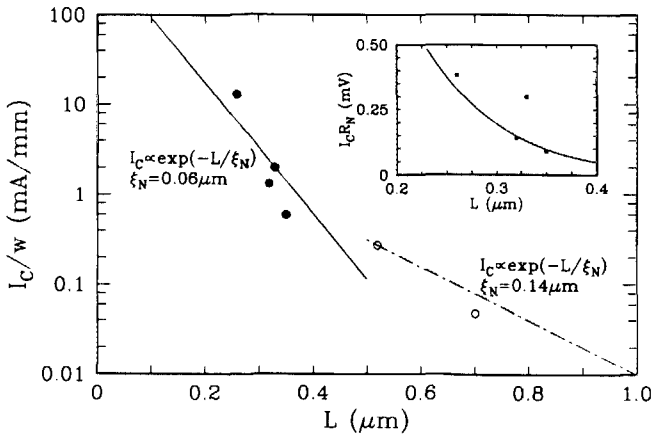

FIG. 2. Critical current (normalized by device width) vs measured link length for $N_D = 3.5\times10^{17}$ cm^{-3}. The solid circles are our data; the open circles are from Ref. 8, for Nb weak links on bulk InAs for a similar doping. The lines, of the form $\exp(-L/\xi_N)$, are drawn through one data point from each experiment, using appropriate values for ξ_N, to illustrate consistency with the expected length dependence. The inset shows the length dependence of the $I_C R_N$ product at 4.2 K. The solid curve is the prediction of Ref. 13; no adjustable parameters are used.

through data points; only the slopes are relevant). The values of ξ_n used were 0.14 μm for the bulk sample[8] (dashed line) and 0.060 μm for our sample (solid line).

The $I_C R_N$ product at 4.2 K is shown in the inset to Fig. 2. The R_N values are the differential resistances at voltages large enough that the I-V's are linear, $\simeq 10$ mV. The solid curve is the theory of Likharev [Eq. (2)], with ξ_N (4.2 K) $= 0.060\,\mu$m and no adjustable parameters. The good agreement with the data is remarkable in that we know of no case in which the full theoretical value of $I_C R_N$ was obtained experimentally for an SNS junction. In fact, there is some argument as to the validity of Likharev's result.[9] Clearly studies of more samples having different dopings would be very useful.

In summary, we have grown thin InAs layers on semi-insulating GaAs substrates with a wide range of dopings and reasonable mobility values. SNS weak link devices fabricated on a 3.5×10^{17} cm^{-3} n-type sample demonstrate that critical currents comparable to those obtained with bulk InAs devices can be achieved, with the advantages of easy device isolation and channel thickness control. Device behavior can be understood with simple SNS weak link theory. The $I_C R_N$ values obtained in this work are quite high, suggesting that semiconductor-coupled Josephson SNS weak links are indeed promising. This structure is intended to be applicable to low voltage FET devices, and should lead to modulation-doped superconducting FET's and other similar devices.

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[1]T. Nishino, M. Miyake, Y. Harada, and U. Kawabe, IEEE Electron Device Lett. **EDL-6**, 297 (1985).
[2]T. Nishino, E. Yamada, and U. Kawabe, Phys. Rev. B **33**, 2042 (1986).
[3]H. Takayanagi and T. Kawakami, Phys. Rev. Lett. **54**, 2449 (1985).
[4]H. Takayanagi and T. Kawakami, *International Electron Devices Meeting Digest* (IEEE, Piscataway, NJ, 1985), p. 98.
[5]A. H. Silver, A. B. Chase, M. McColl, and M. F. Millea, in *Future Trends in Superconductive Electronics*, edited by B. S. Deaver, C. M. Falco, J. H. Harris, and S. A. Wolf (American Institute of Physics, New York, 1978), p. 364.
[6]T. D. Clark, R. J. Prance, and A. D. C. Grassie, J. Appl. Phys. **51**, 2736 (1980).
[7]T. D. Clark, Ph.D. thesis, University of London, 1971 (unpublished).
[8]T. Kawakami and H. Takayanagi, Appl. Phys. Lett. **46**, 92 (1985).
[9]R. B. van Dover, A. de Lozanne, and M. R. Beasley, J. Appl. Phys. **52**, 7327 (1981).
[10]R. C. Ruby and T. van Duzer, IEEE Trans. Electron Devices **ED-28**, 1394 (1981).
[11]A. Serfaty, J. Aponte, and M. Octavio, J. Low Temp. Phys. **63**, 23 (1986).
[12]A. W. Kleinsasser (unpublished).
[13]K. K. Likharev, Pis'ma Zh. Tekh. Fiz. **2**, 29 (1976) [Sov. Tech. Phys. Lett. **2**, 12 (1976)].
[14]S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981), Appendix G.
[15]N. A. Semikolenova, I. M. Nesmelova, and E. N. Khabarov, Fiz. Tekh. Poluprovodn. **12**, 1915 (1978) [Sov. Phys. Semicon. **12**, 1139 (1978)].