Gallium-arsenide deep-level *pin* tunnel diode with very negative conductance

J.L. Pan, J.E. McManis, L. Grober and J.M. Woodall

The first tunnel diodes utilising deep levels in low-temperature-grown gallium arsenide (GaAs) are demonstrated. At room temperature, the negative conductance per area of 1/1.2 kΩ μm^2 is the largest ever measured in GaAs tunnel diodes, which also show peak-to-valley current ratios as high as 19 and peaks of 1.6 kA/cm^2.

Tunnel diodes, which show negative differential conductance (NDC), are important components of amplifiers and oscillators in future high-speed terahertz (THz) systems. The magnitude of the NDC per area determines the maximum attainable frequency of an oscillator. Here we demonstrate the first tunnel diodes utilising deep–levels in low-temperature-grown (LTG) gallium arsenide (GaAs). At room temperature, our NDC per area of 1/1.2 kΩ μm^2 is the largest ever measured in GaAs tunnel diodes, which also show peak-to-valley current ratios as high as 19 and peaks of 1.6 kA/cm^2.

Our sample was grown in an EPI GEN II MBE system on an *n*-GaAs substrate. 1 μm of GaAs was grown at a pyrometer temperature of 550°C at 1 μm/h with an Si doping of 10^{19} cm^{-3} and an As_2-to-Ga flux ratio of 15. The substrate was lowered to 225°C during the growth of 300 nm of GaAs at 0.5 μm/hour and an Si doping of 3.5×10^{18} cm^{-3}. Then came 400 nm of LTG-GaAs at 225°C at 0.5 μm/hour and an Si doping of 3×10^{18} cm^{-3}. The substrate was raised to 350°C during the first 100 nm of a 300 nm layer of unintentionally doped (UID) GaAs. The top layer was 200 nm of GaAs having a Be doping of 10^{20} cm^{-3} grown at 350°C. Standard photolithography steps were used to etch mesas and deposit titanium–gold contacts. The contacts were not annealed. The *p*-contacts were ohmic with a resistance of 2–15 Ω. The *n*-contacts were weak Schottky diodes, requiring 0.6 V to reach mA currents. Radiative emission was measured with a Newport 818IG InGaAs detector.

Current–voltage characteristics for (100 μm)^2 pixels are shown in Figs. 1*a* and *b* and for 40 μm diameter ones in Figs. 1*c* and *d*. At room-temperature, our measured peak-to-valley current ratios are: (*a*) 10, (*b*) 19, (*c*) 10 and (*d*) 19, and the magnitude of our NDC per area correspond to (*a*) 45, (*b*) 6.1, (*c*) 1.2 and (*d*) 1.6 kΩ-μm^2. Our room temperature NDC of 1/1.2 kΩ μm^2 is the largest ever in GaAs tunnel diodes, which also show such large peak-to-valley ratios and large peak densities (1.6 kA/cm^2). The NDC-per-area determines the maximum attainable frequency of an oscillator. The previous best [2] GaAs tunnel diodes have exhibited a room temperature NDC of 1/25.1 kΩ μm^2 at a peak-to-valley current ratio of 28 and peaks of 1.8 kA/cm^2. Our present devices differ from the previous ones [2] in the existence of the LT layer grown at 225°C. Our large negative conductance results from a large density of deep states within a narrow energy range in LT GaAs: 10^{20} cm^{-3} of arsenic-antisite As_{Ga} [1] deep levels at $E_{d1} = 0.75$ eV above the valence band.

Significantly, radiative emission is observed only after the sharp current drops (labelled A) in Fig. 1. This radiative emission indicates the presence of valence band holes and conduction band electrons. The absence of radiative emission at smaller voltages (between zero volts and the points A in Fig. 1) indicates a scarceness of valence band holes and conduction band electrons. This scarceness of free holes and electrons at smaller voltages indicates that carrier transport occurs mainly through the deep level E_{d1}, rather than through the conduction and valence bands.

Fig. 2 shows some possible energy band lineups for our device in forward bias. In Fig. 2, the broken lines indicate quasi-Fermi levels in the P, LT, and N layers. Fig. 2*a* corresponds to the smaller voltages (between zero volts and the points A) in Fig. 1. The positions of the quasi-Fermi levels in Fig. 2*a* emphasise that at these small voltages: (i) most of the applied voltage drops over the Schottky-like *n*-contact, and (ii) carrier transport through the LT layer occurs mainly through E_{d1}, rather than through the conduction and valence bands.

At voltages greater than those of the points A in Fig. 1, some voltage drops across the P–LT–N layers. The voltage at the points labelled F in Figs. 1*a–d* is 1.4 V higher than the voltage at the sharp rises in the current in Figs. 1*a–d*. This 1.4 V corresponds to the bandgap E_G. This indicates that, at the points *F*, a voltage E_G/q drops across the P–LT–N layers. This is the flat band condition, the energy band lineup of which is shown in Fig. 2*f*. At the points F in Figs. 1*a–d*, the current is observed to rise sharply. A large current is indeed expected for the flat band condition.

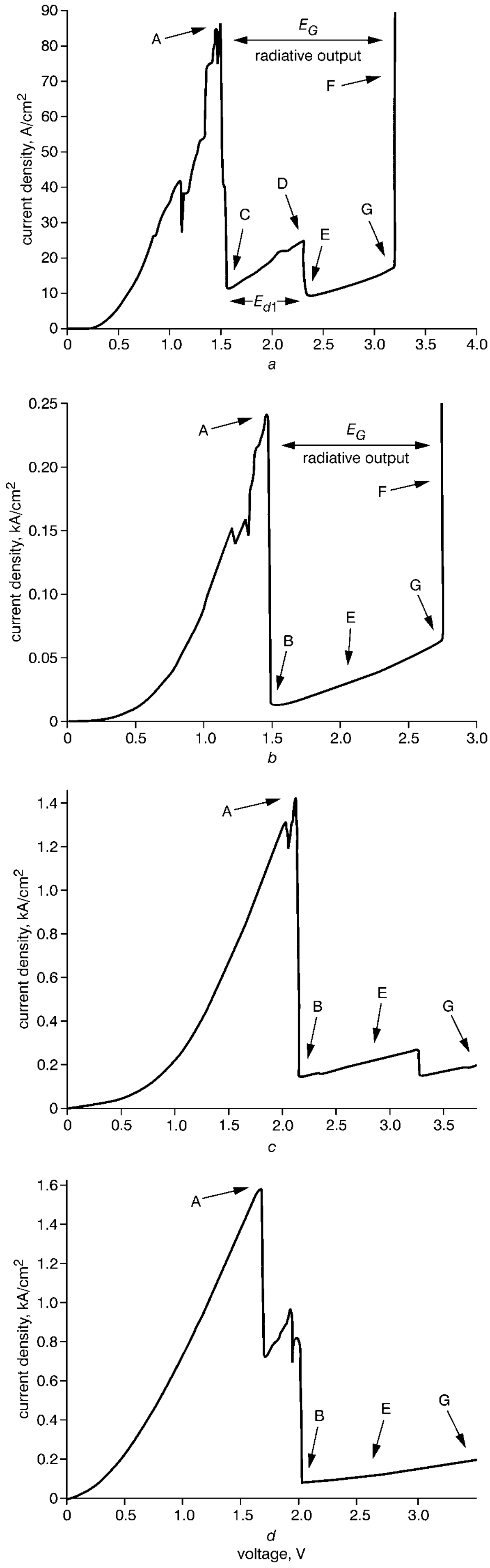

Fig. 1 *Measured current–voltage characteristics*

Our NDC-per-area correspond to *a* 45, *b* 6.1, *c* 1.2, *d* 1.6 kΩ μm^2

Our sample was designed with a UID layer between the P and LT layers, as shown in Fig. 2. Since this UID layer is the most resistive layer in the sample, most of the voltage across the P–LT–N layers will initially drop across the UID layer. This is indicated by the band diagrams in Figs. 2*c* and *d*. Figs. 2*c* and *d* correspond to the points labelled C and D in Fig. 1*a*.

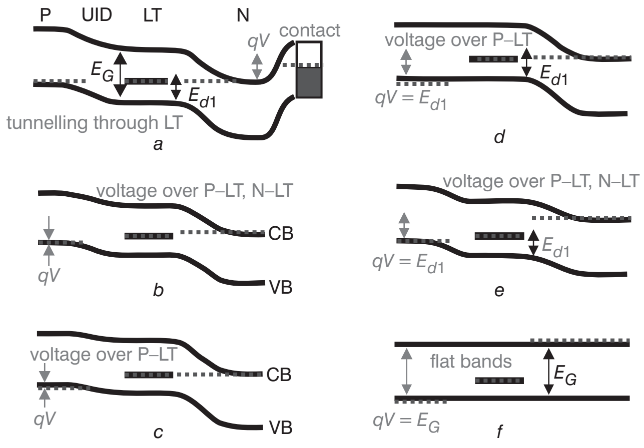

Fig. 2 *Possible energy band lineups for our device in forward bias*

At the points D and E in Fig. 1*a*, the current drops sharply again. The voltage at the points D and E in Fig. 1*a* is 0.75 V higher than the voltage at point A. This 0.75 V is precisely the As_{Ga} deep-level [1] E_{d1} as measured from the valence band edge. The sharp drop in the current from point D to E in Fig. 1*a* indicates a sharp change in the energy band lineup. Points D and E in Fig. 1*a* correspond to the energy band lineups in Figs. 2*d* and *e*, respectively. Although the total voltage between the P- and N-layers is the same E_{d1}/q in both Figs. 2*d* and *e*, most of the voltage drops across the P–LT junction in Fig. 2*d*. Thus, in Fig. 2*d*, E_{d1} in the LT-layer is degenerate with the quasi-Fermi level in the N-layer. The reason the current is higher for Fig. 2*d* (compared with Fig. 2*e*) is that electrons in the N-layer in Fig. 2*d* efficiently tunnel into E_{d1} in the LT-layer, and the valence band of the P-layer in Fig. 2*d* is degenerate with the valence band of the LT-layer. This change in the carrier transport, from elastic tunnelling into E_{d1} from the N-layer in Fig. 2*d* to other mechanisms in Fig. 2*e*, manifests itself in Fig. 1*a* by a sharp change in the differential conductance from a large value (between points C and D) to a small value (between points E and G).

Finally, the differential resistance does not undergo any sharp changes between points B and G in Figs. 1*b*–*d*, unlike Fig. 1*a*. Thus, we expect that the energy band lineup does not change sharply in the entire region between points B and G in Figs. 1*b*–*d*, unlike Fig. 1*a*. Most likely, this is a result of a UID layer, which is not resistive enough. By analogy with points E and G in Fig. 1*a*, the carrier transport mechanism in the entire region between points B and G in Figs. 1*b*–*d* is not dominated by elastic tunnelling into E_{d1} from the N-layer. The band diagrams associated with points B and E in Figs. 1*b*–*d* are shown in Figs. 2*b* and *e*, respectively. Figs. 2*b* and *e* show that significant voltage drops over both the P–LT and LT–N junctions (instead of over the P–LT junction only, as in Figs. 2*c* and *d*). The significant voltage drops over both P–LT and LT–N junctions in Figs. 2*b* and *e* imply that E_{d1} is not degenerate with the quasi-Fermi level of either the P- or the N-layer. Thus carrier transport in Figs. 2*b* and *e* is dominated by mechanisms other than elastic tunnelling into E_{d1} from either the P- or the N-layer. The latter include transport through conduction or valence-bands or deep-levels other than E_{d1}, and phonon-assisted tunnelling through E_{d1}.

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