GaAs metallization: Some problems and trends

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Ohmic and Schottky barrier contacts with desired properties are difficult to form on GaAs devices. This is due mainly to the fact that the position of the Fermi energy is loosely "pinned" near midgap for GaAs surfaces which are metallized using conventional techniques. Doped alloyed metal ohmic and refractory metal Schottky contacts formed on carefully cleaned surfaces are currently widely used. New contacting techniques including the use of lattice matched heterojunctions, nonalloyed n^{++} and p^{++} surfaces, graded band gap structures, and special surface treatment prior to metallization promise to provide both greater flexibility and control for future applications.

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I. INTRODUCTION

One measure of the maturity of a device technology is the ease and reliability of applying contact metallurgy. For most successful and sophisticated metallurgies there usually exists a large and very diverse body of knowledge concerning the detailed behavior of the metal–semiconductor interface. Thus, the maturity of silicon device technologies is easily demonstrated by a perusal of those articles in these proceedings which deal with the metallization of silicon.

In contrast, the status of GaAs metallization is much different, and, to borrow an overworked pun, the surface has barely been scratched. Until recently, very little work had been done on metallizing GaAs integrated circuits. Instead, most GaAs devices such as lasers, solar cells, LEDs, and Gunn diodes were either discrete or monolithic devices for which the demands on metallization were rather modest. For example, the desired contact resistances for these applications are in the range 10^{-1}–10^{-5} Ω cm^2. However, with the advent of the GaAs MESFET and integrated circuits, very stringent requirements were placed on both ohmic and Schottky barrier contacts. For ohmic contacts, a contact resistance of less than 5×10^{-6} is generally required, while a Schottky barrier height tolerance of ± 0.01 V is desired. As researchers worked to achieve these new goals, they discovered that basic information concerning both the metal–GaAs interface and the GaAs surface was lacking. As a result, during the past few years there has been extensive research in the areas of: (1) alloyed doped metal contacts, particularly the Au–Ge–Ni contact in order to lower contact resistances and improve uniformity; (2) the fundamental physics and chemistry of Schottky barrier formation (including ohmic contacts); (3) new techniques for improving and controlling the properties of ohmic and Schottky contacts. This and subsequent papers will briefly review some of the progress in these areas.

II. "IDEAL" CONTACTS

For an ideal metal–semiconductor interface, i.e., one in which the interface is inert and there are no appreciable surface or induced interface states in the semiconductor, the Schottky barrier height is given by[1]

$$\phi_{bn} = \phi_m - \chi_{s.c.}$$

and

$$\phi_{bp} = \frac{E_g}{q} + \chi_{s.c.} - \phi_m,$$

where

ϕ_{bn} = Schottky barrier height to an n-type semiconductor

ϕ_{bp} = Schottky barrier height to a p-type semiconductor

ϕ_m = metal work function

$\chi_{s.c.}$ = electron affinity of the semiconductor

Thus, for example, an "ideal" ohmic metal-n-type-semiconductor contact is one in which $\phi_m \le \chi_{s.c.}$ and $\phi_{bn} \le 0$. Likewise, a rectifying Schottky barrier contact is one in which $\phi_m > \chi_{s.c.}$ and $\phi_{bn} > 0$. Thus, for the ideal case and for a given semiconductor ϕ_b should be determined by the metal work function. Unfortunately, this is not the case for GaAs and many other semiconductors.

III. THE GaAs SURFACE AND INTERFACE—FERMI LEVEL PINNING

When a piece of GaAs is carefully cleaved in ultrahigh vacuum (UHV) conditions, it is found that the position of the Fermi energy level at the (110) cleaved surface is usually the same as the Fermi level in the bulk[2] as shown in Fig. 1. This has also been found for other compound semiconductors as well.[2,3] It has also been shown that when 0.01–0.1 monolayer of different metals or oxygen cover the (110) surface of GaAs and other compounds as well, the Fermi level at the surface becomes "loosely pinned" within a small range of energies, ± 0.1 V, and that the pinning energy is roughly independent of the "contaminating" metal or oxide.[4] For GaAs this pinning position is about 0.8 eV below the conduction band minimum. Since 0.8 eV is roughly the Schottky barrier height most metals

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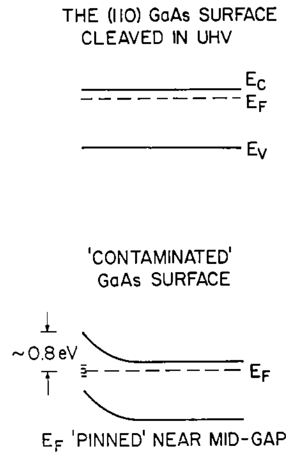


FIG. 1. Schematic band diagram representations of semiconductors with "pinned" and "unpinned" Fermi energy levels at the surface.

make to n-type GaAs[5], and therefore independent of metal work junction, it has been postulated that Fermi level pinning is the fundamental determinate of Schottky barriers. Several models and empirical rules have been proposed to explain pinning. Spicer *et al.*[4] have suggested that pinning is due to surface states induced by the interaction of either metal or oxygen beams with the GaAs surface and that the surface states are associated with native defects, e.g. arsenic and gallium vacancies, produced by the interaction. Surface states have long been associated with Schottky barrier heights. Bardeen showed that a surface state density of $\geq 10^{13}$ cm^{-2} is sufficient to fix the barrier height.[6] Subsequently Mead and Spitzer[5] developed the two-thirds band gap rule based on calculations of expected energies of the surface states. Kurtin *et al.*[7] subsequently showed that semiconductors which were more "ionic" in nature appeared more "ideal", i.e. a lower surface state density, hence $\phi_b = f(\phi_m)$, whereas the more covalent materials showed $\phi_b \neq f(\phi_m)$ behavior. Further studies by McCaldin *et al.*[8] using Au as a reference metal to a variety of p-type compound semiconductors showed that ϕ_{bp} was related to the anion component of the semiconductor and that ϕ_{bp} varied inversely with the anion electronegativity. Since the valence band maximum is due mainly to wave functions of the anion component of the semiconductor, it is suggested that the ϕ_{bp} is tied to the valence band, i.e. a bulk electronic property of the material rather than surface states per se. There are other models which predict Fermi level pinning which also do not invoke surface states. Chemical reactivity of the metal–semiconductor interface has been shown by Brillson to be important in determining the variation in barrier height.[9] It was shown that semiconductors with relatively small heats of formations had barrier heights which were less sensitive to the applied metal than were semiconductors with relatively large heats of formation. The former type of semiconductors are expected to be very reactive with the metal contact and thus the interface composition is expected to dominate the barrier height, whereas the latter type are less reactive and thus the barrier height is expected to be determined by either the metal work function or by interface states induced by the metal.

In spite of the rich array of various models, there are some notable experimental results which remain unexplained. One is the fact that liquid gallium will make a temporary ohmic contact to lightly doped n-type GaAs under the conditions in which the native oxide to GaAs is erupted exposing clean gallium to an oxide free GaAs surface.[10] With time and exposure to air the contact will become rectifying as predicted by previous models. The second and more convincing result is the study by Okamoto *et al.*[11] of Schottky barrier heights for the Al–(GaAs–AlAs) interface prepared by molecular beam epitaxy. They find barrier heights, particularly to AlAs, which are significantly different than those predicted by previous models and which are significantly different than those reported for Au–AlAs.[5] This has led us to propose yet another model which appears at this time to account for a large amount of experimental data including the above observations.

The model is called the Effective Work Function Model, in which the Fermi energy position at the surface (or interface) is not due to or fixed by surface states but rather is related to the work functions of microclusters of the one or more interface phases resulting from either oxygen contamination or metal–semiconductor reactions which occur during metallization. This behavior is shown in Fig. 2. The UHV cleaved (110) surface is free of intrinsic surface states and hence E_F is uniform as seen in the top of Fig. 1. All other surfaces exhibit band bending prior to any intentional surface treatment or metal deposition. The theory requires that these "pinned" surfaces already contain microclusters of interface phases due to their exposure to air or any other surface contaminating environment. When a metal is deposited, there is a region at the interface which contains a matrix of native oxide embedded with microclusters of different phases, each having its own work function. Since the model does not require "surface states", Eq. (1) can be modified and rewritten as

$$\phi_{bn} = \phi_{eff} - \chi_{s.c.}, \quad (3)$$

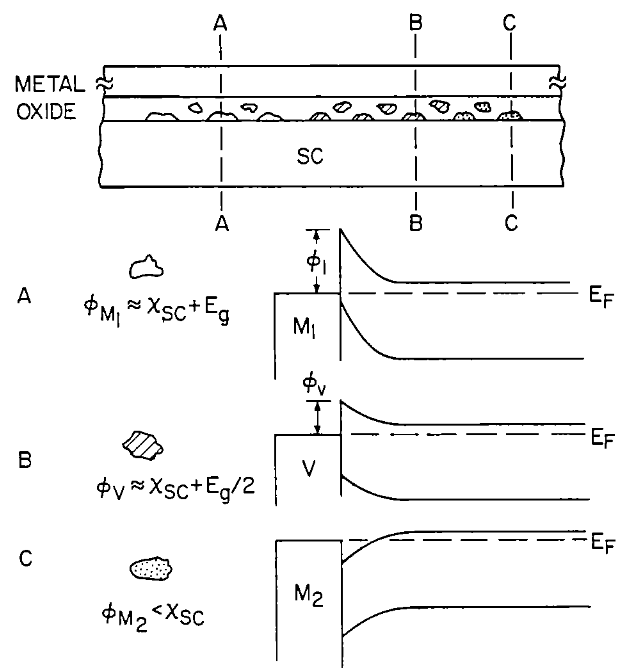
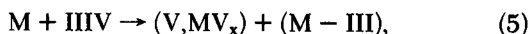


FIG. 2. Schematic representation showing the effects of microclusters of different interface phases on ϕ_{eff} (see text), according to the postulates of the effective work function (EWF) theory. Cross sections "A", "B" and "C" show the barrier heights associated with phases M_1, V, and M_2 of arbitrarily different work functions, respectively.

where ϕ_{eff} is an appropriately weighted average of the work functions of the different interface phases. Thus, the measured ϕ_{bn} can depend somewhat on the measurement technique, i.e. C–V or I–V.

For most of the III–V compounds including GaAs, conventional metallization, i.e. non-UHV conditions, results in a condition in which ϕ_{eff} is due mainly to ϕ_V, the work function of the group V component, and occurs as a result of either one or both of the following reactions:

$$\mathrm{VO} + \mathrm{IIIV} \rightarrow \mathrm{V} + \mathrm{IIIO} \quad (4)$$



$$\mathrm{M} + \mathrm{IIIV} \rightarrow (\mathrm{V},\mathrm{MV}_x) + (\mathrm{M} - \mathrm{III}), \quad (5)$$

where VO + IIIO are generic group V and III oxides and M is a metal.

The conditions for driving the reaction (4) to the right and hence generating excess V at the interface is that the Gibbs free energy, ΔF, is negative. A list of such oxide reactions is shown in Table I.[12] Note that excess group V has been experimentally observed when ΔF is negative, i.e. GaAs, InAs, InSb,[13,14] and that it is not observed when ΔF is positive, i.e. for GaP.[14] It is interesting to note that for InP, $\Delta F \approx 0$, it has been possible to form MISFET structures which exhibit a low interface state density.[15] This is consistent with our model which would predict either no or very little excess free phosphorus at the interface and that the phosphorus would form a positive Schottky barrier to the InP which would act like an interface state within the band gap. Likewise, it should also be noted that for GaAs it is well known that MOSFET structures have notoriously high "interface state densities" (10^{13}–10^{14} cm^{-2}) and that excess arsenic is usually observed at the interface.[16] Again this is consistent with the model since the ϕ_{bn} expected for the As–GaAs interface is about 0.8 eV (the usually observed barrier height for most metal depositions). Since workers have reported a large density of mid-gap states for MOSFET GaAs structures, the model would ascribe these "states" to arsenic clusters at the interface which act as Schottky barrier contacts with $\phi_{bn} \approx 0.8$ eV embedded in an oxide matrix. If the model is correct, a GaP MOSFET structure with low interface state densities would be predicted since no free P is expected at the interface. In addition to oxide reactions, excess group V can be generated by reaction of metals e.g. via reaction (5). For example, it is known that Au deposited on GaAs and GaP results in excess Ga in the Au film.[17] Also, preliminary phase diagram data[18] shows that an arsenic phase is expected at equilibrium for Au–GaAs and

TABLE I. IIIV + VO → IIIO + V (e.g., 2GaAs + As_2O_3 → Ga_2O_3 + 4As).

	ΔF
AlP	(−) Large
GaP[a]	(+) Small
InP	(~) 0
AlAs	(−) Large
GaAs[b]	(−) Large
InAs[b]	(−) Large
AlSb	(−) Large
GaSb[b]	(−) Large
InSb	(−) Small

[a] Excess V not observed at interface
[b] Excess V observed at interface

TABLE II[a]. Au–IIIV Schottky barriers.

Does $\phi_{Au} = \chi_{s.c.} + \phi_{bn} = 5.1$–$5.5$ eV?			
IIIV	ϕ_{bp}	$\chi_{s.c.} + \phi_{bn}$	ϕ_V
GaP	0.96	4.9	5.0
InP	0.85	4.9	5.0
AlAs[b]	0.9	4.7-5.1	5.0 (4.8)[d]
	(1.4)[c]	(4.2-4.6)[c]	(ϕ_{Al} = 4.0-4.2)
GaAs	0.5	5.0	5.0 (4.8)[d]
InAs	0.3-0.5	4.8-5.0	5.0 (4.8)[d]
AlSb[b]	0.54	4.7	4.8 (4.7)[d]
GaSb	0.1	4.7	4.8 (4.7)[d]
InSb	~0.1	4.8 (77 K)	4.8 (4.7)[d]

[a] See Refs. 2, 11, 19, 27–37
[b] Does not obey common anion rule
[c] Al–AlAs barriers
[d] Measured values (Ref. 37)

Au–InSb. Thus, a knowledge of both oxide and reactive metal chemistry should enable accurate predictions of the transport properties of metal–IIIV devices (e.g. observed Schottky barrier heights). The current status of the predictive ability of the model for IIIV compounds is in Table II, which lists the experimentally derived values of ϕ_{bp} and $\chi_{s.c.} + \phi_{bn}$ for Au–IIIV contacts. There are three points to note in this table. First, the equation

$$\phi_{Au} = \chi_{s.c.} + \phi_{bn} = 5.1\text{–}5.5 \text{ eV} \quad (6)$$

is not obeyed for all the III–V compounds. Second, the common anion rule is not obeyed for AlAs and AlSb. Third, the EWF model agrees well, as expected, for $\phi_{eff} = \phi_V$, i.e. $\phi_V = \phi_{bn} + \chi_{s.c.}$ except, as expected, for the Al–AlAs result.[11] For the Al–AlAs case, this metallization was annealed and performed in a UHV MBE system where the Al and AlAs surface was very clean. Thus, it is expected that ϕ_{eff} should be dominated by $\phi_{Al} = 4.0$–4.2 eV. Thus, since $\chi_{s.c.} + \phi_{bn} = 4.2$–$4.6$ for this case is much closer to ϕ_{Al} than to ϕ_{As} or ϕ_{Au} we believe that ϕ_{bn} is due mainly to ϕ_{Al}. Similarly the Ga–GaAs ohmic contract mentioned earlier can be explained since $\phi_{Ga} = 4.36$ eV[19] and $\phi_{bn} = 0$–0.3 (for ohmic behavior); $\chi_{GaAs} + \phi_{bn} = 4.1$–$4.4 \approx \phi_{Ga}$.

IV. HETEROJUNCTION CONTACTS

Fortunately, there are ways to circumvent the problem of uncontrolled Schottky barrier heights. One of the most widely used methods is the lattice matched heterojunction. When two semiconductor materials with nearly equal lattice constants form an epitaxial interface, predictable interface transport properties are observed provided very abrupt junctions can be formed and one material does not dope the other. An example is the $Ga_{1-x}Al_xAs$–GaAs interface, shown schematically in Fig. 3. When the electron affinities are different, $\chi_A \neq \chi_B$, a rectifying Schottky barrier with a controlled barrier height is formed (Fig. 3). When $\chi_A \approx \chi_B$ ohmic behavior is observed. This situation is thought to occur for the n-Ge/n-GaAs interface[20]; however, there is some chance that the ohmic behavior could be due to n^+ doping of the GaAs side of the interface by Ge. Another method for forming ohmic contacts to GaAs and also avoiding the Fermi level pinning problem is shown in Fig. 4. Figure 4(a) shows the "conventional"

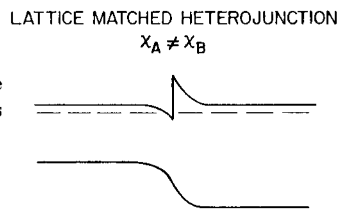


FIG. 3. Band diagram of a lattice matched heterojunction of materials with different electron affinities.

metal–GaAs contact with $\phi_{bn} \approx 0.8$ eV. For doping levels below 5×10^{17} rectifying Schottky barrier behavior is observed. In order to make an "ohmic" contact for this situation, it is necessary to form an n^+ layer between the metal and the n-type semiconductor which allows electrons to tunnel through the barrier. Figure 4(b) shows the analogous situation for the metal/n-InAs contact. In this case, the Fermi level is pinned *in* the conduction band. Thus, there is no barrier ($\phi_{bn} \leq 0$) to electron flow and the contact is ohmic. Figure 4(c) shows the case for an abrupt interface between n-InAs and n-GaAs with a metal on the InAs. Note that E_F is pinned at the same position as for the metal–GaAs case. This is due to the fact that there is a large lattice constant mismatch between GaAs and InAs which causes a large density of misfit dislocations to form at the interface which, in turn, pins E_F in both the GaAs and InAs. This problem is overcome by forming a nonabrupt interface by grading the interface region from GaAs to InAs as shown in Fig. 4(d). This structure has been shown to have a low contact resistance, $<10^{-6}\ \Omega\,\text{cm}^2$, for nonalloyed metal contact to the InAs.[21]

V. SURFACE TREATMENT

There are cases where a specialized surface treatment has been found to significantly alter Schottky barrier heights. For example, the n-GaAs-electrolyte interface barrier height is significantly different when the GaAs surface is treated with $RuCl_3$ and the electrolyte is strongly basic and contains S^- and $S^=$ ions.[22] More recently, it has been shown that the *in situ* H_2S treatment of n-type GaAs grown by MBE prior to room deposition of Al results in an apparent reduction of the barrier height and has been attributed to a reduction in the surface state density.[23]

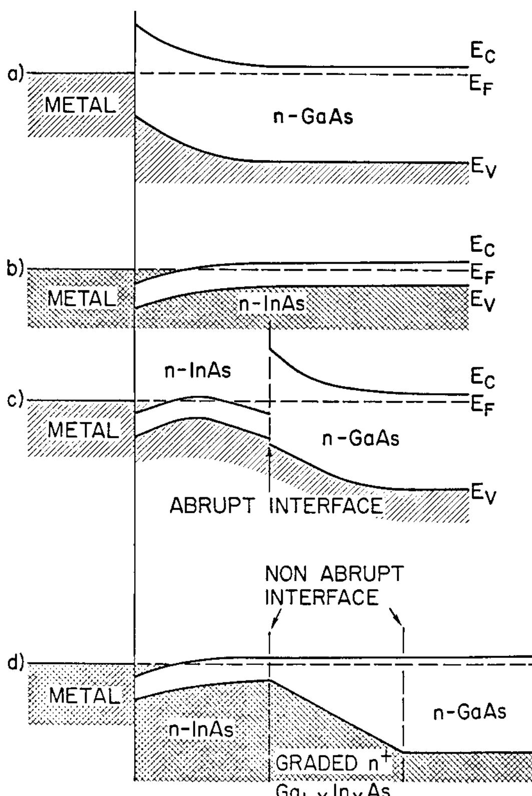


FIG. 4. Band diagram representation of different types of metal-semiconductor interfaces and structures.

VI. CONVENTIONAL CONTACTS

Currently, metallization specialists are coping with Fermi level pinning using doped metal alloyed contacts for forming ohmic contacts and using non or slightly reactive refractory metal Schottky barrier contacts. The ohmic "work horse" has been the Au–Ge–Ni contact which will be discussed in detail in a subsequent article. Of all the current Schottky barrier contacts, the Ti/W metallurgy appears to be the most promising because of its high temperature stability.[24] Ion implantation[25] and MBE[26] are being developed to form n^+ surface layers in order to eliminate the uncontrolled alloyed contact. It is clear, however, that the future of GaAs large scale integration depends on a better understanding of the metal–GaAs interface, especially the chemistry of the interface phases.

VII. SUMMARY

The electrical behavior of most metal–GaAs interfaces is dominated by the apparent pinning of the Fermi energy level at the GaAs surface at a value of about 0.8 eV. Various theories explain this behavior in terms of (1) surface states due to native defects in the semiconductor; (2) chemical interactions between the metal and semiconductor; (3) the energy of the valence band of the semiconductor; and (4) the effective work function of one or more interface phases. Device technologists are currently coping with this phenomena for discrete and monolithic devices using doped alloy metal ohmic and refractory metal Schottky barrier contacts. However, it is not certain that these technologies will be adequate for the manufacture of GaAs integrated circuits. Lattice matched heterojunctions and graded band gap structures, along with n^+ doping techniques appear to be viable solutions for this problem.

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