Summary Abstract: Surface treatment and interface properties: What really matters?

J. M. Woodall and J. L. Freeouf

IBM Thomas J. Watson Research Center, New York 10598

(Received 1 February 1984; accepted 24 April 1984)

PACS numbers: 81.60. – j, 73.40. – c, 68.90. + g, 68.48. + f

There has been much recent progress on both the theoretical understanding of the electronic structure of idealized III–V semiconductor surfaces and interfaces and the UHV characterization of real surfaces and interfaces. However, except for a few cases, this knowledge is insufficient to adequately explain the optical and electrical behavior of surfaces and interfaces used in practical devices. For example, information obtained from monolayer and submonolayer depositions in UHV conditions on cleaved (110) surfaces, although useful, does not lead to a fundamental understanding of such device properties as Schottky barrier height, Ohmic contact resistance, and surface recombination velocities. One reason for this is that the interpretation of UHV results is complicated by the difficulty of differentiating between metallurgical, e.g., interface chemistry, and structural, e.g., surface defects, effects which occur simultaneously during deposition. Another reason is that practical devices are made on (100) surfaces whereas most of the UHV work has been on (110) surfaces, and it is well known that the "clean" versions of these surfaces are both structurally and electronically different. Finally, there are problems in relating the experimental results of measurements such as I–V, C–V, XPS, and photoemission to concepts such as barrier height, electron affinity, work function, surface states, and surface energy levels.

Let us compare some interface models with experimental data, especially with respect to the variation of surface and interface properties with surface treatment. We know, for example, that GaAs(110) surfaces formed by cleaving in UHV are free of surface states which lie in the direct gap.[1] Thus, the Fermi level at the surface is the same as that for the bulk. Theory and experiment are reconciled on this issue. To date it appears that all other gas or vacuum/GaAs surfaces have a surface Fermi level which is pinned roughly at midgap. In fact, the results of UHV experiments on (110) surfaces with submonolayer coverage of a variety of adatoms suggest that there may be two levels, a deep acceptor and a deep donor, which are associated with surface defects which are responsible for the pinning.[2] It has been known for some time that Schottky barriers to GaAs cannot be directly explained by the Schottky work function model, i.e., the barrier height is not proportional to the work function of the applied metallurgy. This coupled with the UHV pinning results has led to the hypothesis that the fundamental mechanism of Schottky barrier formation for metal/GaAs interfaces used in solid state devices is Fermi level pinning due to surface defects.[3] At first glance this model appears compelling since the pinning positions are within 0.1 eV of the barrier heights commonly quoted in textbooks. However, there is a problem with reconciling the predictions of a two energy level, i.e., two pinning position, surface defect model with experimental observations that in some cases, the sum of the p-type and n-type barrier heights equals the band gap energy. A recent attempt[4] to resolve this problem shows that in order to reconcile these observations with the defect models, a surface defect density of at least 0.1 monolayers is required. At this density the barrier height is only a weak function of the metal work function. Therefore, the observed midgap barrier heights can be explained by juggling the deep level defect density and the metal work function.

Thus, it is beginning to appear that barrier heights at metal/GaAs interfaces can be explained in terms of a coupled interaction between the electronic properties of a dominant surface effect, e.g., vacancies, antisite defects, clusters, MIGS, surface reconstruction, etc., and the electronic properties of the applied metallurgy, e.g., the work function. The task is to identify the dominant surface effect(s) and to relate their occurrence to surface preparation and metallization method. The nature of the dominant surface effect is by no means resolved. There are many observations which tend to rule out deep level surface vacancies or antisite-type defects as the dominant surface effect.[5] For example, the Pd/GaAs interfaces for which the Fermi level is not at pinned midgap.[5] Furthermore, for the two level defect models, two distinct regions of almost constant barrier height (each corresponding to one pinning defect) should be observed as a function of the metal work function.[4] This may have been seen for InP,[6] but not for GaAs as yet. There are, in fact, observed barrier heights, e.g., for Al/AlAs formed by MBE,[7] which are adequately explained by the simple work function model, i.e., the Al work function and AlAs electron affinity, and with no defect levels required. Also, there is the following paradox: (1) it takes 0.1 monolayers of deep level defects to pin the Fermi level at midgap and produce the observed barrier heights; (2) these defects are produced by metallization from thermal beams; (3) the Schottky barriers, and hence the defect density, are stable to an 800 °C anneal; (4) this surface defect density corresponds to a volume density of 10^{21} cm^{-3}; (5) layers grown by the MBE method using thermal beams have volume defect densities of only 10^{13} cm^{-3} or less. How is this defect density reduced by eight orders of magnitude for MBE grown layers and not for annealed metal/GaAs interfaces? Thus, a theoretical framework which requires the surface effects to be deep, multileveled, and of opposite conductivity type seems too restrictive in view of the wide var-

iety of experimental results. Also, metal induced gap state models are not sufficiently developed to explain the wide range of observed barrier height for a given material.

An alternative framework is the effective work function model,[5,8] in which the Fermi energy position at the surface (or interface) is not due to or fixed by surface defects or surface states but rather it is related to the work functions of microclusters of the one or more interface phases resulting from contamination, e.g., exposure to air, or to reactions which occur during metallization. The theory requires that "pinned" surfaces already contain microclusters of interface phases. According to the model when a metal is deposited, for example, to an air exposed surface, there is a region at the interface which contains a matrix of native oxide embedded with microclusters of different phases, each having it own work function. Thus, the normal work function model is rewritten as

$$\phi_{bn} = \phi_{\text{eff}} - x_{s.c.},$$

where ϕ_{eff} is appropriately weighted average of the work functions of the different interface phases. Thus, the measured ϕ_{bn} can depend somewhat on the measurement technique, i.e., C–V or I–V. In other words, the interface phases comprise the Schottky barrier contact. The rest of the bulk metallurgy has little or no effect on the barrier height, except when the interface phases are predominantly the same as the applied metallurgy, e.g., Al/AlAs interfaces formed by MBE.

For most of the III–V compounds including GaAs, conventional metallization, i.e., non-UHV conditions, results in a condition in which ϕ_{eff} is due mainly to ϕ_{V}, the work function of the group V component, and occurs as a result of either one or both of the following reactions:

$$\text{VO} + \text{IIIV} \rightarrow \text{V} + \text{IIIO},$$

$$\text{M} + \text{IIIV} \rightarrow (\text{V},\text{MV}_X) + (\text{M},\text{III}),$$

where VO + IIIO are generic group V and III oxides and M is a metal. Using this framework we are able to explain the usual midgap pinning related Schottky barrier heights, the anomalous barriers, e.g., the Al/AlAs interface and the Pd/GaAs interface, where the sum of the n- and p-type barrier heights is much less than the band gap, and the properties of MIS structures.[5,8]

However, determining the proper framework is not enough. In order to impact metal/semiconductor device technology we must attend to details. A chip with an array of ten thousand gates requires a threshold voltage variation of less that 20 mV. This translates into a barrier height variation of less than 20 mV. We are not aware of any model/theory, unified or specific, capable of this resolution. A specific model with this resolution which relates I–V determined barrier heights to surface treatment and deposition condition for a single useful metallurgy to GaAs would be a major contribution and greatly welcomed by the device processing community. However, it is quite possible that this problem is too complicated to be addressed by our current knowledge and experimental capabilities. This is particularly true in view of the fact most of our current knowledge of GaAs surfaces is based on UHV studies of (110) surfaces, whereas devices are predominantly made on (100) surfaces which have not been observed in an unpinned condition. The (110) surface is nonpolar (containing equal numbers of As and Ga atoms in each plane) and is known to reconstruct by relaxation mechanisms which do not alter the surface symmetry or unit cell; the (100) surface is highly polar, possibly containing only As or Ga atoms in a single plane, and is known to exhibit many reconstructions involving large surface unit cells. Epitaxial growth is known to be easier on (100) surfaces, especially by MBE; attempts at growth on (110) surfaces typically leads to morphological and (for alloys) clustering phenomena. Such distinctions in surface structure and growth phenomena could well correlate with metallurgical interactions, which in turn would impact several of the Fermi level pinning models currently under discussion.

With regard to semiconductor heterojunctions it appears that from a practical point of view the common anion and electron affinity rules are adequate to explain trends in the optical and electronic behavior of properly formed lattice matched or pseudomorphic isoelectronic heterojunctions.[9] Nearly all other heterojunction interfaces used in electronic devices, including those containing misfit dislocations,[9] can be approximated by Fermi level pinning models in combination with doping effects. However, by device fabrication standards, adequate theoretical tools have not yet been developed for these interfaces. Thus, there is a need for a microscopic interface theory for device structures with parameters which can be both measured by existing experimental procedures and related to important device parameters.

[1]J. Van Laar, A. Huijser, and T. L. Van Rooy, J. Vac. Sci. Technol. **14**, 894 (1977).
[2]W. E. Spicer, I. Lindau, P. Skeath, and C. Y. Su, J. Vac. Sci. Technol. **17**, 1019 (1980).
[3]W. E. Spicer, I. Lindau, P. Skeath, and C. Y. Su, Appl. Surf. Sci. **9**, 83 (1981).
[4]A. Zur, T. C. Mcgill, and D. I. Smith, Surf. Sci. **132**, 456 (1983); Phys. Rev. B **28**, 2060 (1983).
[5]J. M. Woodall and J. L. Freeouf, J. Vac. Sci. Technol. **19**, 794 (1981).
[6]R. H. Williams, J. Vac. Sci. Technol. **18**, 929 (1981).
[7]K. Okamoto, C. E. C. Wood, and L. F. Eastman, Appl. Phys. Lett. **38**, 636 (1981).
[8]J. L. Freeouf and J. M. Woodall, Appl. Phys. Lett. **39**, 727 (1981).
[9]J. M. Woodall, G. D. Pettit, T. N. Jackson, C. Lanza, K. L. Kavanagh, and J. W. Mayer, Phys. Rev. Lett. **51**, 1783 (1981).