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THE ELECTRONIC PROPERTIES AND CONTROL OF SEMICONDUCTOR INTERFACES

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ABSTRACT

Much progress has been made towards the understanding and elimination of the Fermi level pinning problem at compound semiconductor surfaces and interfaces. This progress includes the discovery of several new techniques for reducing and controlling the surface state density and the achievement of metal work function dominated barrier heights at metal/(100) GaAs interfaces. This paper will review this work and the relevance of various Fermi level pinning theories to these results.

INTRODUCTION

The development of compound semiconductor devices has been hampered by the presence of an appreciable density of uncontrolled surface states, whose origin is still a topic of controversy. These states tend to "pin" the location of the Fermi level at various kinds of semiconductor interfaces at some characteristic energy. This pinning adversely affects the performance of both high speed and optoelectronic devices and circuits. The introduction of the lattice matched heterojunction in 1967 by Woodall and Rupprecht (1) became the basis of a partial solution to the "Fermi level pinning" problem for many optoelectronic devices, e.g. LEDs, DH lasers, solar cells, etc., and for some high speed devices, e.g. HEMTs and HBTs. Nonetheless, the Fermi level pinning problem still hampers the development of other desirable devices such as MOSFETs, the optimization of metal contacts, and the passivation of devices and circuits.

FERMI LEVEL PINNING

Fermi level pinning is manifest in several ways. The two most notable are the insensitivity of the Schottky barrier height to metal workfunction (2) and the large density of interface states seen, for example, in GaAs MOS structures (3). Pinning theory can be classified into two groups, Fermi level pinning as an intrinsic property of the semiconductor related to either bulk or surface band structure (4,5), e.g. MIGS or some variant, or Fermi level pinning as an extrinsic property of the semiconductor related to native defects, (6), disorder, (7), or anion phase workfunction (8). It is interesting to note that to date only Duke and Mailhot, (9) and Freeouf and Woodall, (8) have explicitly stated that in the absence of extrinsic Fermi level pinning, the Schottky workfunction limit should be the dominant mechanism for locating the interface Fermi level. Most of the other extrinsic pinning models have tacitly assumed that pinning is inevitable due to the technological aspects of forming a semiconductor interface, i.e. the deposition of either a metal layer (6) or a dielectric film (7) causes pinning. To describe this situation in philosophical terms, except for Woodall and Freeouf (8), there was but dim hope that either metal workfunction dominated barriers or dielectric interfaces with a low surface state density could ever be achieved. However, this situation changed abruptly in 1986 when the IBM group (10) reported that light-induced

photochemistry between both n and p type (100) GaAs and water (photowash) greatly reduced the surface state density.

TECHNIQUES FOR PRODUCING LOW SURFACE STATE DENSITY

Photowashed GaAs

In the photowash (PW) method the GaAs surface is illuminated with greater than band gap energy photons at an intensity on the order of 10 Watts cm ^{2} The light source is typically either an ELH tungsten halogen 300 W projector bulb or an argon ion laser (488 nm). During the photon illumination the GaAs is mounted on a photoresist type "spinner" and flushed with D.I. water for a period which can be varied from between 10 and 10^{3} seconds. As a result of this treatment it has been previously shown (11-13) that the GaAs surface is passivated with an oxide layer whose chemistry is predominately Ga_2O_3 with only a trace of As_2O_3 , and whose thickness is an increasing function of photowash time. For the case of PW generated oxides of > 5 nm thickness, a "photoactivation" step after PW is necessary to reduce the band bending so that increased PL will be seen (11,12). Evidence for a reduced interface state density includes: increased band edge photoluminescence (PL) (10,14), a reduced surface recombination velocity (15,16,17), C-V characterization (10), and the photoreflectance modulation of the surface electric field (18).

In spite of the many positive indications that the PW technique leads to GaAs with a low surface state density and hence more nearly flat band, PW experiments by Hasegawa (15) have resulted in surfaces with increased band bending, as indicated by resistance measurements on ungated FET structures which have had the PW treatment. As a consequence of ref. 15 the present authors performed the experiment shown in Fig. 1. The GaAs structure is basically an n/p photovoltaic device in which PL, the short circuit current, and sheet resistance of the top n-layer can be monitored during the PW treatment. As shown in Fig. 1, and unlike reference 15, we find a decrease in sheet resistance after PW. This decrease in sheet resistance correlates with an increase in both the PL and short circuit current and is consistent with the notion of decreased band bending, surface state density, and hence the elimination of Fermi level pinning as far as device applications are concerned.

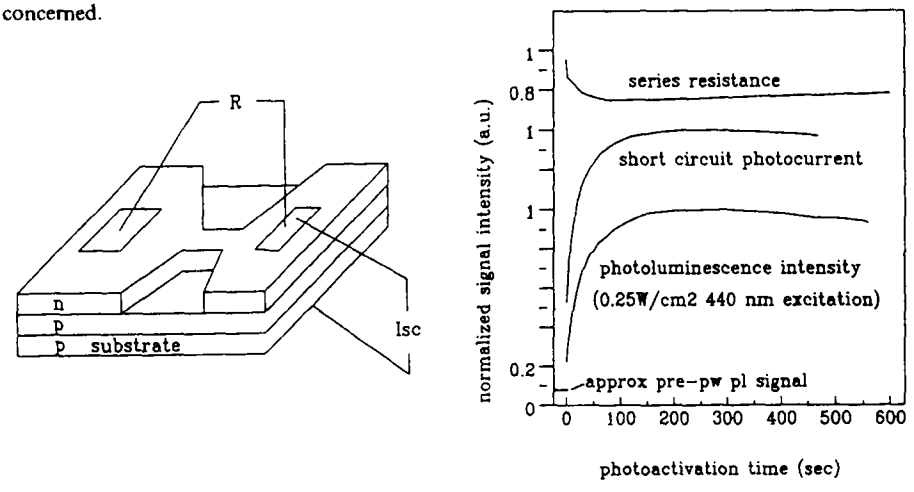

Fig. 1. Photoluminescence, short circuit current, and sheet resistance for n/p photovoltaic structure before and after photowash treatment (see text). All data are normalized to unity for maximum values.

It should be noted that thick oxides produced by the PW method are quite porous and that repinning occurs in air within several hours. Thus, it is very unlikely that these oxides will have useful applications in device technology. It may be possible to use thin PW oxide layers as part of unpinned MOS structures in conjunction with other dielectric materials. However, the most important aspect of this work is its impact on previous notions concerning Fermi level pinning. We have shown that Fermi level pinning is indeed an extrinsic feature of the dielectric/GaAs interface and that a dielectric layer can be formed on GaAs which does not cause pinning. Furthermore, the chemistry of the PW formed gallium oxide/GaAs interface offers convincing evidence in support of a conclusion of the effective work function (EWF) model (8), that the presence of excess elemental anion, e.g As, and elemental anion generating oxides, e.g. As_2O_3, causes Fermi level pinning and that the elimination of these components would produce unpinned interfaces.

The Sulfide Techniques

About a year after the report of the photowash results a group at Bellcore (16) reported on an alternative technique for greatly reducing the GaAs surface recombination velocity. In their technique the native oxides are first removed from the GaAs surface. This is followed by spin coating the surface with a film of $Na_2S{\cdot}9H_2O$. Compared with the PW technique the sulfide film has been shown to impact device technology more directly, e.g., by improving the gain of HBT's (19). An ammonium sulfide treatment has been shown to both reduce the surface leakage component in p/n junction diodes (20) and to provide a greater range in Schottky barrier heights than for surfaces with native oxide (21). Other tests demonstrating unpinning include PL studies (22,23) and carrier lifetime studies (16). The PL studies of refs. 12 and 23 reveal that the behavior of the PW and sulfide layers are very similar. The detailed chemical studies reveal that the sulfide passivated layers are such that the GaAs surface is either terminated by gallium rich sulfides (24,25) or by an arsenic sulfide compound (26). In all cases, unpinning, like the case for the PW treatment, is associated with the removal of the arsenic components in the native oxide prior to forming the sulfide layer. This result also supports the EWF model of Fermi level pinning.

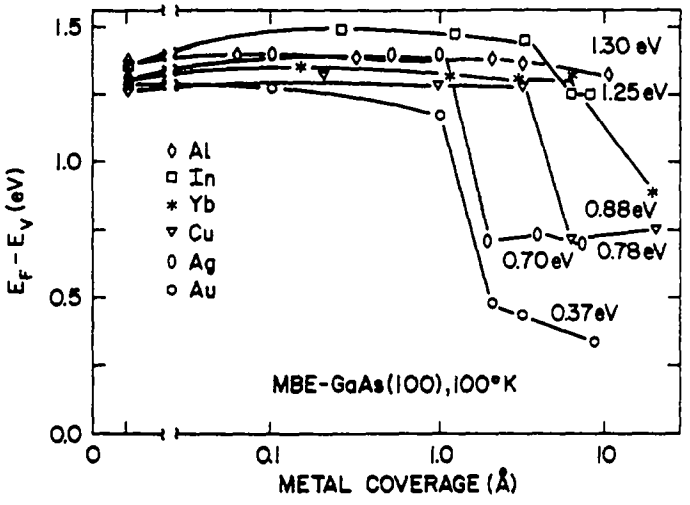

Fig. 2. E_f movements as a function of metal coverage for Ag, Al, Au, Cu, In, and Yb deposited at 100K on n-type MBE grown GaAs and measured by soft x-ray photoemission.

The UHV GaAs (100) Surface with the (2x4) Reconstruction

Recently, the atomic structure of the (100) GaAs (2x4) reconstruction has been determined by scanning tunneling microscopy (STM) (27). The STM images show that the 4x periodicity is due to a regular array of missing arsenic dimers. This structure had been predicted by Chadi to have minimum energy (28). The calculations also predict a forbidden gap of this reconstruction to be larger than for bulk GaAs. This suggests fewer gap states and no inherent Fermi level pinning. A key to obtaining the STM result was the use of an As capping layer and desorption technique developed by a Rockwell group (29) to protect an MBE grown surface during transit to the STM apparatus. This same technique was used by the Xerox-Wisconsin-IBM group to prepare flat band n-type GaAs prior to metal deposition (30). Again, this result is constant with the EWF model and the Chadi prediction. The results of the metallization of these surfaces will be discussed below.

The Pseudomorphic Interface Control Layer

It is well known that compound semiconductor heterojunctions such as GaAlAs/GaAs and GaInAs/GaAs formed free of interface defects do not exhibit Fermi level pinning. Recently (31,32,33) a technique utilizing this knowledge was developed to form an unpinned interface between GaAs and SiO_2 for the purpose of forming MIS structures with a low interface state density. The technique called the interface control layer (ICL) (33) consists of a structure of GaAs or GaInAs/Si/SiO_2 in which the idea is that the pseudomorphic Si/GaAs will be unpinned and the Si/SiO_2 using Si oxide technology will also have a low interface state density. There is still some controversy about validity of this concept for GaAs. However, it seems to offer some improvements using GaInAs (33). An alternative to the Si ICL, recently shown by the IBM group (34), is the pinning control layer using gallium-group VI compounds, e.g. gallium sulfide.

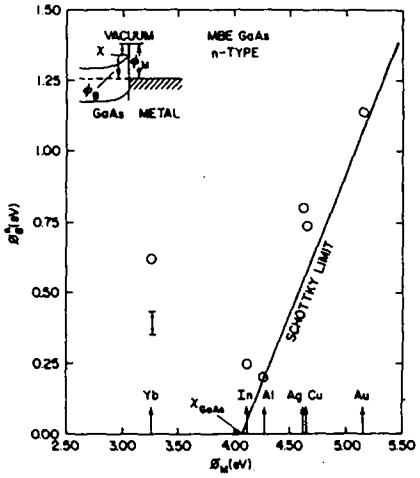

Fig. 3. Experimental Schottky barrier heights from the data in Fig. 2. The solid line is the plot of ϕ_b vs $\phi_m - \chi$. χ = 4.07 eV.

SCHOTTKY LIMIT BARRIERS TO METAL/(100) GaAs INTERFACES

As a culmination of a multi-year Xerox-Wisconsin-IBM joint project, Schottky limited barriers have been observed at metal/(100) GaAs interfaces (30). A summary of recent results are shown in Figs. 2 and 3. In Fig. 2 it should be noted that the As capped and desorbed (100) n-type GaAs starts out flat band prior to metal deposition which is similar to the case for UHV cleaved (110) GaAs. But in contrast to the metallization of (110) surfaces, the behavior of the surface Fermi level

for unpinned (100) surfaces is mostly insensitive to metal coverage until the one monolayer regime is reached. After about one monolayer coverage, the interface Fermi level approaches that expected for the Schottky workfunction limit, i.e., $\phi_b = \phi_m - \chi$. χ = 4.07 eV, (see Fig. 3). It should be noted that the barrier height for Yb is that expected from the workfunction of arsenic. This is not surprising since Yb is expected to be highly reactive with GaAs, and, thus it is expected that elemental As will be generated at the Yb/GaAs interface. Since Fig. 3 shows both pinning and Schottky limited behavior it is very difficult to reconcile this situation with models other than the EWF model (8). It is clear that, for the (100) GaAs used in this study, Fermi level pinning is not an intrinsic phenomena, thus, we can rule out all of the MIGs type models for this case. More recently (35) we have attempted to explain why the metal/(100) GaAs interface is not addressed by MIGs type physics. Our answer is shown schematically in Fig. 4. We hypothesize that the (2x4) or other non-metallic surface reconstructions act like an "insulating" "I" layer of a MIS like structures which isolates the GaAs bulk from the effects of MIGs. This notion is currently being studied in greater detail.

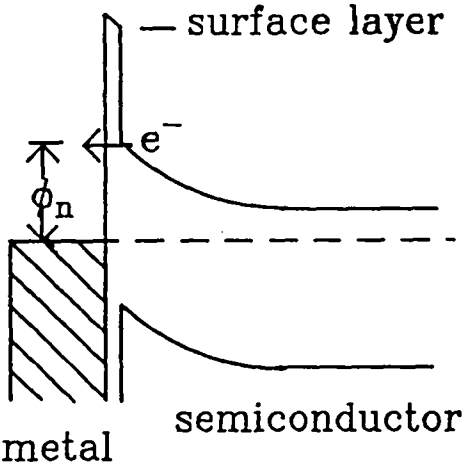

Fig. 4. Schematic illustration of suggested MIS model of unpinned Schottky barriers on GaAs (100). The surface reconstruction is assumed to act as an insulator to prevent Fermi level and is assumed to persist under the metal.

SUMMARY

We have reviewed some recent progress made towards forming unpinned GaAs surfaces and interfaces. We have shown that dielectric/GaAs interfaces can be formed with greatly reduced interface state densities. We have also shown that a metal/(100) GaAs interface can be formed which exhibits Schottky limited barriers in contrast with previously observed pinned interfaces. These results taken together can be consistently explained by the EWF model.

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