Transistors with an emitter area S_E of 1 × 15μm (Fig. 1) were fabricated using the self-aligned process described in [7]. The WSi emitter and Au/Pt/Ti/Mo/Ti/Pt base electrodes were separated by a 0.3μm wide SiO_2 sidewall. The collector electrode was Au/Ni/W/AuGe. The spacing between the emitter electrode and the poly-GaAs under the base electrode was 1.1μm.

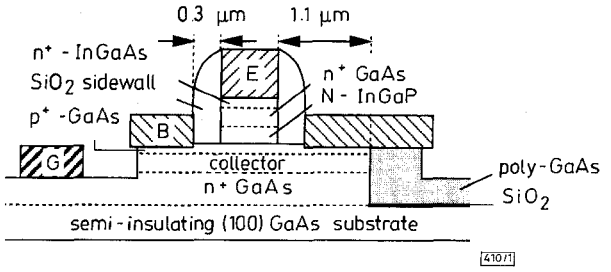

Fig. 1 *Schematic illustration of cross-section of InGaP/GaAs LBCT with poly-GaAs buried under base electrode*

Gummel plots for transistors with and without poly-GaAs were almost identical, and current gain exceeded 17 at a collector current density of 6×10^4 A/cm^2. Capacitance measurements showed that C_{BC} at zero bias was 34fF for a transistor with poly-GaAs, while it was 39fF for a transistor without poly-GaAs. This C_{BC} reduction is attributed to complete carrier depletion in the poly-GaAs under the base electrode.

Fig. 2 shows frequency against current gain h_{21}, Mason's unilateral gain U, and maximum stable gain (*MSG*) for transistors with and without poly-GaAs. The *s*-parameters were measured under the condition of a collector-emitter bias of 1.6V and a collector current of 10mA. Although our f_T of 170GHz is almost the same as the f_T in [2], our measured f_{max} of 170GHz is double that in [2] due to a larger base doping (1×10^{20}cm^{-3} against 4×10^{19}cm^{-3}).

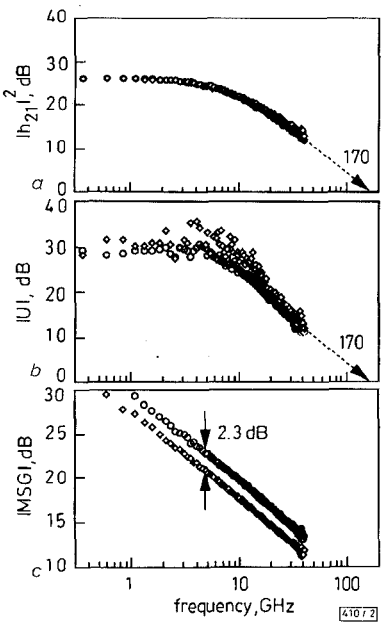

Fig. 2 *Dependences of current gain h_{21}, Mason's unilateral gain U, and maximum stable gain MSG on frequency for transistors with and without poly-GaAs*

Emitter area 1 × 15μm; collector-emitter bias 1.6V; collector current 10mA
○ with poly-GaAs
◇ without poly-GaAs

Although no difference appeared in the f_T and f_{max} between transistors with and without poly-GaAs, the *MSG* of a transistor with poly-GaAs was 2.3dB higher than that of a transistor without poly-GaAs. This increased *MSG* came from the reduction in extrinsic C_{BC}. This result agrees with an analytical treatment of *MSG* by Kurishima [8].

In conclusion, we have achieved a high f_{max} of 170GHz by heavy C-doping and an *MSG* increase of 2.3dB by using buried poly-GaAs.

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Low-temperature grown GaAs tunnel junctions

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Indexing terms: Gallium arsenide, Tunnelling

A GaAs tunnel junction is formed by molecular beam epitaxy at low substrate temperatures to incorporate excess arsenic, followed by an anneal to precipitate the excess arsenic. This tunnel junction is comparable in resistance and peak current density to tunnel junctions grown stoichiometrically. Owing to the inhomogeneity in this two-phase tunnel junction, there is only a slight indication of a current peak. This lack of a valley in the tunnelling characteristic results in a low voltage drop even for currents in excess of the peak current.

Non-alloyed, low-resistance, tunnelling contacts can be readily made to *p*-GaAs since accepter concentrations of up to 1×10^{20} cm^{-3} are acheivable. Non-alloyed contacts are significantly more problematic to *n*-GaAn because, as silicon concentrations are increased, the silicon starts to substitute on arsenic sites compensating the material and limiting the net electron concentration to 5×10^{18}cm^{-3} [1]. We are interested in non-alloyed contacts to both *p*- and *n*-GaAs for application to thin light-emitting diodes where alloying into the GaAs, or alloying after substrate removal, would be detrimental, and where a good optically reflecting contact is desired [2]. A *p*-GaAs region could be used for contact on both sides of the diode with the incorporation of a tunnel junction between the *n*-side of the diode and the *p*-GaAs contact layer. Tunnel junctions are also useful as embedded electrical connections in other structures such as tandem solar cells [3]. In this Letter, we describe a novel technique to form a GaAs tunnel junction and use it to electrically short a *p*-$Al_{0.3}Ga_{0.7}As$ layer to an *n*-$Al_{0.3}Ga_{0.7}As$ layer.

Our approach to GaAs tunnel junctions centres on molecular beam epitaxy (MBE) at low-substrate temperatures, ~250°C, in order to incorporate 1% excess arsenic in the tunnel region [4]. This excess arsenic will precipitate with anneal resulting in a two-phase system of semi-metallic arsenic precipitates in a GaAs matrix [5]. The Schottky barrier height between the arsenic precipitates and the GaAs matrix is 0.7eV [6]. If arsenic precipitates can be formed in the junction region, a two-step process would be possible with the electrons tunnelling from the valence band on the *p*-side to an arsenic precipitate and then from the arsenic precipitate to the conduction band on the *n*-side. This two step tunnelling process, with tunnelling barriers of ~0.7eV, should be more efficient than tunnelling directly between the valence and conduction bands with a tunnelling barrier of 1.42eV. A further benefit of the low-temperature growth is to ensure higher substitutional donor concentrations for silicon and acceptor concentrations for beryllium [7, 8]. The resulting reduced concentration of interstitial beryllium, because of the low-temperature growth, should result in less dopant diffusion [7], a concern with tunnel junctions because of the high doping concentrations.

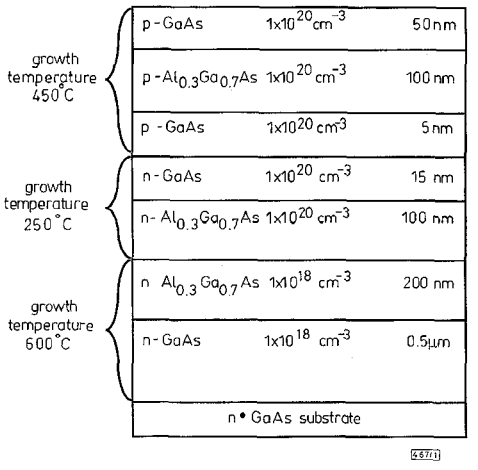

Fig. 1 *Cross-section of tunnel junction structure*

In non-stoichiometric GaAs, after the excess arsenic has precipitated with anneal, further anneal or higher temperature anneal will result in a coarsening of the arsenic precipitates [9, 10]. The driving force for this coarsening is a reduction in the arsenic precipitate to GaAs matrix surface area and hence surface energy. The precipitation and coarsening process can be strongly influenced by doping and the presence of heterojunctions. At a *pn*-junction the arsenic precipitates will form on both the *n*- and *p*-sides, but preferentially coarsen from the *p* to *n*-side [7, 10]. Because of the electric field, asenic precipitates will quickly coarsen out of the depletion region of a *pn* junction [7, 10]. This would result in a quick removal of precipitates from the junction region and loss of the two-step tunnel process. At AlGaAs/GaAs heterojunctions, the arsenic precipitates preferentially coarsen to the lower bandgap GaAs regions [10, 11]. This preferential coarsening is driven by the lower interfacial energy of an arsenic precipitate in GaAs than in AlGaAs, because the Ga-to-As bond is weaker than the Al-to-As bond. AlGaAs barriers could concievably reduce the loss of arsenic precipitates from the depletion region of the GaAs tunnel junction.

Our tunnel junction structure is shown in Fig. 1. The tunnel region consisted of 7nm of *p*-GaAs (1×10^{20}cm^{-3}) and 16nm of *n*-GaAs (1×10^{20}cm^{-3}). Cladding the tunnel region on top is a *p*-$Al_{0.3}Ga_{0.7}As$ region, and on the bottom an *n*-$Al_{0.3}Ga_{0.7}As$ region. The *p*-GaAs and *p*-$Al_{0.3}Ga_{0.7}As$ regions were grown at 450°C so that very little excess arsenic would be incorporated while the temperature is sufficiently low to prevent diffusion or precipitation of the excess arsenic in the tunnel junction region. The part of the *n*-$Al_{0.3}Ga_{0.7}As$ region closest to the *n*-GaAs was grown at 250°C to provide an additional source of excess arsenic to the GaAs tunnel region, in an attempt to compensate for the loss of arsenic caused by the electric field in the depletion region. The back-side contact to the *n*-GaAs substrate was alloyed indium and the top contact was a non-alloyed Ti/Au tunnelling contact to a heavily doped *p*-GaAs contact layer.

The current-voltage (IV) characteristics of a $240 \times 380\mu m^2$ tunnel junction are shown in Fig. 2*a* for different anneal conditions. The anneals were for 30s at temperatures ranging from 600 to 900°C. For as-grown, the structure exhibited non-ohmic behaviour. In the as-grown structure, the excess arsenic is in the form of point defects: arsenic antisites and interstitials, and gallium vacancies. For an anneal of 600°C for 30s, the excess arsenic is just beginning to nucleate into precipitates, and there is very little change in the IV characteristic. With a higher temperature anneal there is a dramatic change in the IV characteristic as the excess arsenic precipitates. After a 700°C 30s anneal, a tunnelling characteristic was observed with a specific resistivity of $1.2m\Omega\text{-}cm^2$ and a peak current density of 95A/cm^2, although there was just a hint of a peak current believed caused by inhomogeneity in the structure. A tunnelling characteristic was also observed after anneals at 750 and 800°C, with a slight increase in the specific resistivity and a decrease in the peak current density. After a 900°C anneal, the IV characteristic reverted to rectifying with a high turn-on voltage indicative of the $Al_{0.3}Ga_{0.7}As$ *pn* junction. This rectifying IV characteristic observed for the 900°C annealed sample is due to arsenic precipitate coarsening, precipitates moving out of the depletion region, and dopant diffusion at the *pn* junction. A more complete IV characteristic for the 900°C annealed sample is shown in Fig. 2*b*, along with the IV characteristic for the as-grown sample and the 700°C annealed sample.

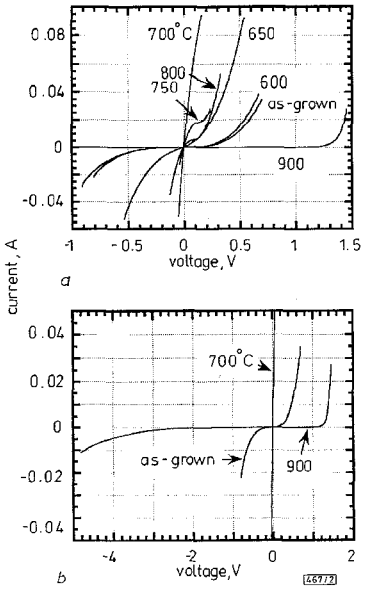

Fig. 2 *Current-voltage characteristics of 240 × 380μm² tunnel junction for different anneal conditions*

In conclusion, we have demonstrated a GaAs tunnel junction formed by MBE at low substrate temperatures to incorporate excess arsenic followed by an anneal to precipitate the excess arsenic. The peak current density of our tunnel junction is significantly higher and more stable, since a 700°C anneal is used to form the junction, than previously demonstrated tunnel junctions grown by MBE [12, 13]. The resistance and peak current density of our tunnel junction compares favourably to those grown by metal-organic chemical vapour deposition [14 – 16]. Because of the inhomogeneity in our two-phase tunnel junction, there is only a slight indication of a current peak after the 700°C anneal. Because of the lack of a valley in the tunnelling characteristic, this contact retains a low voltage drop even for currents in excess of the peak current.

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