

# InAs/InGaP/GaAs heterojunction power Schottky rectifiers

A. Chen, M. Young and J.M. Woodall

A low-temperature (LT) grown InAs epi-layer has been applied as the gate to the dual-material structure of lattice-matched InGaP on GaAs, to make a high-temperature power rectifier. The LT molecular beam epitaxy technique enables the formation of an abrupt interface between InAs and InGaP. This heterojunction rectifier utilises the strong thermal stability of the InAs/InGaP heterojunction and the high figure-of-merit of the InGaP/GaAs dual-material structure for power devices. The LT-InAs/InGaP/GaAs heterojunction rectifier demonstrates lower on-state resistance, lower off-state leakage current, and higher breakdown voltage, than metal/GaAs Schottky rectifiers.

**Introduction:**  $\text{In}_{0.49}\text{Ga}_{0.51}\text{P}$  has been shown to have the highest figure-of-merit (FOM) for high-power applications among the commonly used III–V compound semiconductors [1] owing to its wide bandgap ( $\sim 1.9$  eV), high mobility ( $\sim 3000$   $\text{cm}^2/\text{Vs}$ ) and high breakdown electric field ( $\sim 0.8$  MV/cm). One of the objectives of power rectifiers is to reduce the power dissipation by minimising the on-state resistance. InGaP has a FOM of 37 normalised to that of silicon (Si) as 1, indicating that the on-resistance of an InGaP rectifier will be 37 times smaller than that of a Si rectifier. The rectifier on-resistance could be further reduced by 2–3 times in a dual-material structure of lattice-matched InGaP on GaAs [2]. By placing a high critical field material layer on top of a high mobility material layer, the InGaP/GaAs dual-material structure leverages both the high critical field of InGaP and the high mobility of GaAs. The structure was designed so that the top InGaP layer supported the highest electric field in the structure and the electric field at the InGaP/GaAs interface is lower than the critical field of GaAs. An optimised InGaP/GaAs structure has a FOM approximately 60 times better than that of Si. The improved FOM of the dual-material structure was confirmed on a metal-gate Schottky rectifier built on the InGaP/GaAs structure [2].

However, Schottky rectifiers with metal gates tend to degrade severely at high temperatures owing to metallurgical reactions at the metal–semiconductor (M–S) interface [3]. Since power devices are frequently exposed to high-temperature environments or joule heating during operation, thermal stability is a critical concern for M–S Schottky power rectifiers. Recently, it has been demonstrated that heavily doped InAs is highly conductive and can be used as a ‘metal’ layer on another semiconductor to form a rectifying contact [4, 5]. The InAs-gate heterojunction rectifiers have stronger thermal stability than M–S rectifiers, which is attributed to the covalent bonding between two semiconductors and the highly lattice mismatched hetero-interface that effectively blocks impurity diffusion and chemical intermixing [4, 6]. However, an earlier attempt of growing InAs on InGaP by regular molecular-beam epitaxy (MBE) technique led to a non-abrupt interface and leaky contact. Recently, a low-temperature (LT) MBE technique has been developed to form abrupt heterojunction interfaces, and it has been applied to the epitaxy of InAs on GaP and InGaP [6]. The InAs/GaP and InAs/InGaP heterojunction rectifiers were stable after the heat treatment up to 700°C [4, 6].

In this Letter, we demonstrate a power rectifier with an InAs-gate grown by the LT-MBE technique on the InGaP/GaAs dual-material structure, for high-temperature applications. The sample structure is shown in Fig. 1a.

**Experimental:** Although InGaP/GaAs is a lattice-matched structure, there exists a band offset between InGaP and GaAs, which causes additional on-resistance and undermines the advantage of using a dual-material structure [2]. The band offset creates a depletion region in the InGaP layer and an accumulation region in the GaAs. The energy barrier  $\Delta E_C$  (0.15–0.3 eV) inhibits the carrier transportation under forward bias. To solve this problem, a  $\delta$ -doping in the InGaP layer, i.e. a very high doping concentration ( $1 \times 10^{20}$   $\text{cm}^{-3}$ ) in a very thin layer (5 nm), was used at the InGaP/GaAs interface. The  $\delta$ -doping layer could reduce the depletion region thickness in the InGaP layer and enable the tunnelling of carriers through the barrier, which minimises the additional on-resistance.

The LT-InAs/InGaP interface was also modified to achieve desirable barrier height between InAs and InGaP. In the growth of InGaP on

GaAs, an In-rich condition was used to ensure the lattice-match of InGaP to GaAs. In addition, the InP–GaP pseudo-binary system is highly lattice mismatched. The two factors may result in the phase separation in InGaP and produce micro regions on the InGaP surface with 75% InP and 25% GaP, which will form lower Schottky barrier height in contact with InAs. Therefore, a 10 nm thick Ga-rich InGaP surface layer (composition of 55% Ga and 45% In) was grown at the LT-InAs/InGaP interface to compensate for this effect. The second interface modification is to employ a thin layer of heavily doped  $p$ -type LT-InAs (5 nm) at the LT-InAs/InGaP interface to increase the interface band bending, by aligning the Fermi level in InGaP to the valance band edge of InAs.

5 nm, $n$ -type $\text{In}_{0.75}\text{Al}_{0.25}\text{As}$ , $1 \times 10^{19}$ $\text{cm}^{-3}$
50 nm, $n$ -type LT (250°C) InAs, $1 \times 10^{19}$ $\text{cm}^{-3}$
5 nm, $p$ -type LT-InAs, $1 \times 10^{19}$ $\text{cm}^{-3}$
10 nm, $n$ -type $\text{Ga}_{0.55}\text{In}_{0.45}\text{P}$ , $2 \times 10^{16}$ $\text{cm}^{-3}$ (Ga-rich surface)
1.1 $\mu\text{m}$ , $n$ -type $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ , $2 \times 10^{16}$ $\text{cm}^{-3}$
5 nm, $n$ -type $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}$ , $1 \times 10^{20}$ $\text{cm}^{-3}$ ( $\delta$ -doping)
1.6 $\mu\text{m}$ , $n$ -type GaAs, $2 \times 10^{16}$ $\text{cm}^{-3}$
0.5 $\mu\text{m}$ , GaAs buffer layer
$n^+$ -GaAs substrate
a
2.0 $\mu\text{m}$ , $n$ -type GaAs, $2 \times 10^{16}$ $\text{cm}^{-3}$
0.5 $\mu\text{m}$ , GaAs buffer layer
$n^+$ -GaAs substrate
b

**Fig. 1** MBE sample structures

a LT-InAs/InGaP/GaAs heterojunction rectifier

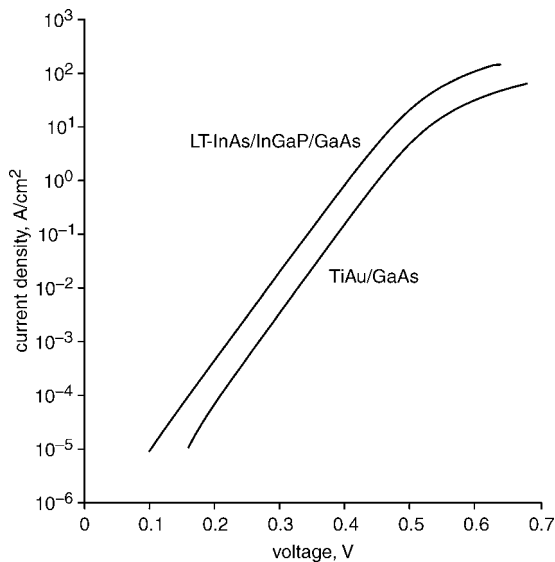
b Metal/GaAs rectifiers

The heterojunction rectifier sample was grown by a solid source MBE. A 1.6  $\mu\text{m}$  thick GaAs epi-layer doped to  $2 \times 10^{16}$   $\text{cm}^{-3}$  with Si is grown on a GaAs substrate with a 0.5  $\mu\text{m}$  thick buffer layer, followed by a 1.1  $\mu\text{m}$  thick InGaP layer doped also by Si to  $2 \times 10^{16}$   $\text{cm}^{-3}$  with  $\delta$ -doping at the InGaP/GaAs interface. Then an LT-InAs layer doped to  $1 \times 10^{19}$   $\text{cm}^{-3}$  was grown above the InGaP, with the two interface modifications mentioned earlier. The InAs layer was capped by  $\text{In}_{0.75}\text{Al}_{0.25}\text{As}$  to minimise the evaporation at high temperatures. A GaAs epi-layer with the same doping concentration ( $2 \times 10^{16}$   $\text{cm}^{-3}$ ) was also grown to fabricate metal/GaAs Schottky rectifiers for comparison, as shown in Fig. 1b.

TiAu was deposited with an e-beam evaporator on the GaAs sample as the metal gate of M–S Schottky rectifiers and on the heterojunction sample as the metal contact. The lift-off process was used for metal patterning. Heterojunction rectifiers were fabricated by etching InAs in  $1\text{H}_2\text{O}_2:3\text{H}_3\text{PO}_4:50\text{H}_2\text{O}$  with the TiAu metal pattern as the etching mask, to form the InAs-gate. The backside ohmic contact on  $n^+$ -GaAs was made of AuGeNi alloyed at 400°C for 30 s in a rapid thermal annealer (RTA).

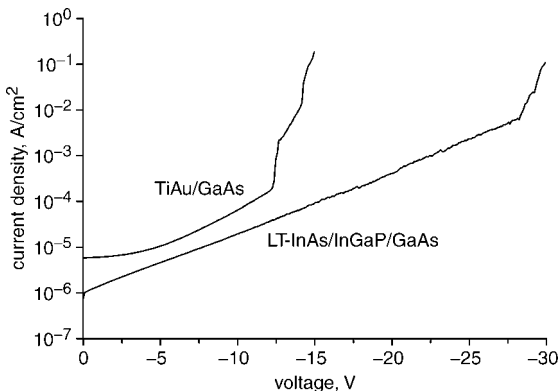
**Results:** Current–voltage (I–V) characteristics were measured using a HP4156A parameter analyser. Fig. 2 shows the forward bias I–V characteristics of the LT-InAs/InGaP/GaAs heterojunction rectifier, in comparison with the TiAu/GaAs Schottky rectifier. The heterojunction rectifier demonstrates nearly ideal Schottky rectifier characteristics, with linear I–V characteristics over six orders of magnitude of current on a semi-logarithmic scale. By fitting the I–V characteristics to the thermoionic emission-diffusion theory, we calculated the ideality factor and the barrier height as 1.03 and 0.82 eV, respectively. The barrier height is slightly improved from the previous result on the LT-InAs/InGaP heterojunction without interface modifications [6]. The on-state current of the heterojunction rectifier is more than six times higher than that of the TiAu/GaAs rectifier, which is desirable for high-power applications. By comparing Fig. 2 with the forward I–V characteristics of the dual-material InGaP/GaAs structure without  $\delta$ -doping [2], it can be seen that the

$\delta$ -doping effectively reduced the additional on-state resistance caused by the InGaP/GaAs band offset.



**Fig. 2** Forward-bias current–voltage characteristics of LT-InAs/InGaP/GaAs heterojunction rectifier and TiAu/GaAs rectifier

The reverse bias I–V characteristics of these two rectifiers are shown in Fig. 3. The heterojunction rectifier shows lower leakage current and higher breakdown voltage than the metal/semiconductor rectifier. The maximum parallel plane electric field achieved is about 0.5 MV/cm on the LT-InAs/InGaP/GaAs rectifier and 0.3 MV/cm on the TiAu/GaAs rectifier, similar to the values reported before on the InGaP/GaAs structure and GaAs [2].



**Fig. 3** Reverse-bias current–voltage characteristics of LT-InAs/InGaP/GaAs heterojunction rectifier and TiAu/GaAs rectifier

The I–V characteristics show that the LT-InAs/InGaP/GaAs heterojunction structure has improved the performance of high-power rectifiers over a single material structure. It has been demonstrated before that heterojunction rectifiers with LT-InAs gates have much stronger thermal reliability than metal-gate rectifiers and could maintain the rectifying characteristics after heat treatment up to 700°C [6].

**Conclusions:** A power rectifier has been made on a dual-material structure of lattice-matched InGaP/GaAs with an InAs-gate grown by the LT-MBE technique. It utilises the strong thermal stability of the LT-InAs/InGaP heterojunction and the superior FOM of the InGaP/GaAs structure.  $\delta$ -doping was employed to minimise the additional on-state resistance caused by the band offset at the InGaP/GaAs interface. The InAs/InGaP interface was modified to achieve desirable barrier height and the effect of these modifications still needs further investigation. This LT-InAs/InGaP/GaAs dual-material heterojunction rectifier appears to be a promising candidate for high-temperature and high-power applications.

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A. Chen and M. Young (*Department of Electrical Engineering, Yale University, New Haven, CT 06511, USA*)

E-mail: an.chen@aya.yale.edu

J.M. Woodall (*School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907, USA*)

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