Field-effect transistors on molecular beam epitaxy GaP

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Field-effect transistors (FETs) were fabricated on epitaxial GaP grown using molecular beam epitaxy. Both metal-semiconductor junctions and *p-n* junctions were tested as gate structures for metal-semiconductor FET and junction FET, respectively. The fabricated FETs demonstrate typical transistor characteristics with low gate leakage that is desirable for low-noise applications. The measured device characteristics match the theoretical expectation based on the material properties of epitaxial GaP and suggest directions for improvement. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2710476]

Gallium phosphide (GaP) is one of the most commonly used III-V compound semiconductors. With a wide band gap of 2.26 eV, it has been considered a promising candidate for high-temperature electronics.[1–3] The extremely low thermal generation rate in GaP can be utilized to make a charge storage device with long retention time.[4] Recently GaP avalanche photodiode has been investigated for low-noise photodetection in the blue/UV spectrum.[5] GaP has demonstrated strong resistance against photocorrosion in aqueous solutions, a property desirable for devices in medical and environmental applications.[6] Closely lattice matched to Si (lattice mismatch ~0.4%), GaP holds high promise in the integration of compound semiconductors on the Si substrate.[7,8] Significant advantages that GaP has over other wide band gap semiconductors for commercial applications are the mature processing technology from prior light-emitting diode work and the low cost of high-quality substrates. The most prevalent growth technique employed for bulk GaP is high-pressure liquid-encapsulated Czochralski.[9] Device quality epitaxial layers have been produced with liquid phase epitaxy,[2,3] vapor phase techniques,[10] and metal-organic chemical-vapor deposition.[11] Recently, molecular beam epitaxy (MBE) has been increasingly explored for the growth of high-quality GaP epilayers. This letter reports the fabrication and characteristics of field-effect transistors (FETs) on epitaxial GaP grown with MBE.

GaP transistors, especially FETs, are important components in the fabrication of monolithic GaP circuits or subsystems for the applications mentioned above. However, the research effort on GaP FET has been very limited and usually focused on specific applications, e.g., high-temperature electronics.[1–4] The metal-oxide-semiconductor FET structure dominant in the Si technology does not exist for GaP, due to the lack of high-quality gate insulators. The quality of native oxides on GaP formed by either thermal oxidation or anodic reaction is insufficient for device applications.[12,13] Synthesized gate dielectrics on GaP still need further improvement on the interface properties for enhancement-mode metal-insulator-semiconductor FET.[14] More feasible gate structures for GaP FETs are metal-semiconductor (MS) Schottky junction and *p-n* junction for metal-semiconductor FET (MESFET) and junction FET (JFET), respectively. In addition to the simplicity in device fabrication, as majority carrier devices, they are also favored in speed consideration and are expected to be inherently radiation hard. Therefore, we have focused on these two FET structures in this work. Since the applications of GaP devices usually utilize its wide band gap and low intrinsic carrier concentration, GaP FETs should demonstrate low gate leakage that is desirable for low-noise performance.

The samples were grown using a solid-source MBE. A 0.4 μm thick *n*-type GaP epilayer doped to 1×10^{17} cm^{-3} was grown on a *p*-type GaP substrate, with a semi-insulating layer between them. The buffer layer isolates the *n* layer (channel) from the substrate and also prevents the impurity diffusion from the substrate into the channel layer. In the sample for JFET, a p^+ layer doped to 5×10^{19} cm^{-3} was grown on top of the *n* layer as the gate structure. The heavy p^+ doping was designed to limit the depletion region mainly in the *n* layer, as well as to facilitate the formation of Ohmic contact on the gate mesa.

The source/drain (*S*/*D*) contacts in MESFET and JFET were made by depositing a Ge–Au/Ni/Au (250–500 Å/300 Å/500 Å) metal stack using an e-beam evaporator and alloying it at 400 °C for 30 s in the N_2 ambient in a rapid thermal annealer. For MESFET, the MS rectifier gate was formed after the *S*/*D* contacts. Both Ni and Cr have been investigated as gate metals. Cr/GaP Schottky barrier has been proven to be stable at high temperatures.[1] Ni was chosen because of its large work function that could increase the band offset and reduce the gate leakage current. For JFET, the p^+ layer was etched to form the gate mesa before the deposition of the *S*/*D* metal contacts on the *n* layer. Finally, nonalloyed Ti/Au (500 Å/1000 Å) was deposited on the patterned p^+ layer to form the Ohmic contact to the gate.[15] The patterning of both Ge–Au/Ni/Au and Ti/Au contacts used the lift-off process. Etching of GaP for JFET gate patterning and the final device isolation was done in $HCl(36\%):HNO_3(65\%):H_2O$ (1:1:1 in volume ratio). To achieve a stable and uniform etching rate, the etching chemical was stabilized for 1 h after mixing and the etching was done with continuous stirring. The etching rate is approximately 4–5 nm/s at room temperature.

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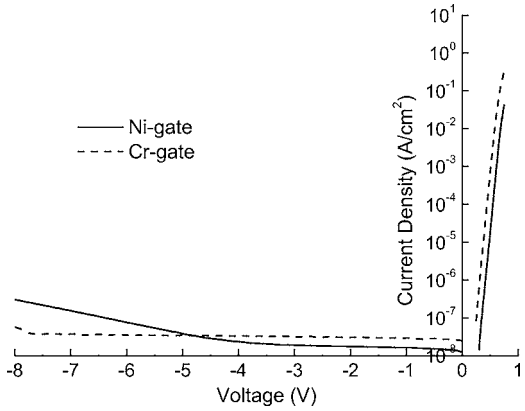

FIG. 1. Gate current-voltage (*I-V*) characteristics of Ni- and Cr-gate GaP MESFETs on semilogarithm scale.

Figure 1 shows the gate current-voltage characteristics of the Ni- and Cr-gate MESFETs. Both gate structures demonstrate nearly ideal Schottky junction characteristics, with the ideality factor of 1.10 for Ni gate and 1.11 for Cr gate. The barrier heights of the Ni gate and Cr gate are calculated to be 1.16 and 1.06 eV, respectively. The barrier height does not reflect the work function difference between Ni and Cr (~0.7 eV), which is likely related to the Fermi level pinning at the metal/GaP interface. The low reverse leakage current density of both junctions (~10–100 nA/cm^2 before breakdown) is desirable for low-noise applications. Owing to the wide band gap and low intrinsic carrier concentration, GaP Schottky junctions are expected to have a significantly lower leakage than Si devices. The MESFET gate *I-V* in Fig. 1 was measured on an on-chip coaxial testing structure, with a ring contact on *n*-GaP around the MS junction. Since the current transport is predominantly horizontal from the MS junction to the peripheral Ohmic contact, the measured leakage current is affected by the high-field edge of the depletion region. As a result, the measured leakage could be much higher than what would be expected from the intrinsic limit of a vertical GaP junction.

GaP *p-n* junction provides a larger barrier height than that of MS junctions and may be more suitable for the reverse bias operation of the depletion-mode FET gate. Figure 2 shows the reverse bias leakage of the gate *p-n* junction of a GaP JFET, with the gate voltage from −5 up to −20 V. The forward bias *I-V* characteristics are shown in the inset. The

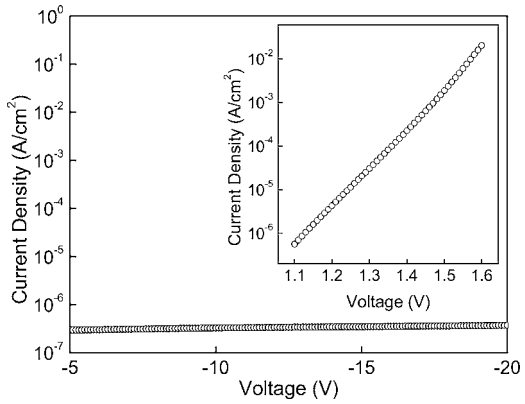

FIG. 2. Reverse bias leakage level of the GaP JFET gate *p-n* junction; inset shows the forward bias current-voltage (*I-V*) characteristics of the gate *p-n* junction.

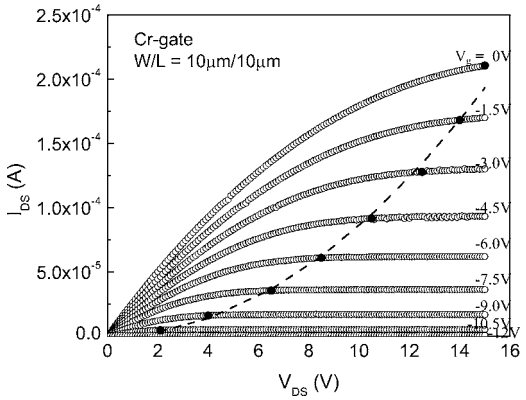

FIG. 3. Channel current-voltage (I_{ds} vs V_{ds}) characteristics of Cr-gate GaP MESFET at different gate voltage V_g's (from 0 to −12 V), with gate width/length ratio of 10 μm/10 μm; dashed line shows fitting to the empirical $I_{dsat} \sim V_{dsat}$ equation.

gate leakage level is low throughout the measurement voltage range. At the reverse bias of −20 V, the maximum electric field in the *p-n* junction depletion region approaches 0.85 MV/cm. Such high field is already beyond the Si material limit (~0.3 MV/cm) but is still below the breakdown field of GaP (~1 MV/cm). Similar to the MS junctions in MESFET, the edge leakage in the horizontal test structure probably dominates the measured gate leakage of JFET. The forward *I-V* characteristics show an ideality factor of 1.8, indicating increasing contribution of the generation-recombination (*G-R*) current in the *p-n* junction.

GaP MESFET and JFET demonstrate similar transistor characteristics. Typical channel current-voltage (I_{ds} vs V_{ds}) characteristics of a Cr-gate GaP MESFET for different gate voltage V_g's are shown in Fig. 3 as an example. The same characteristics were also observed in Ni-gate MESFET. The channel width/length (W/L) ratio here is 1/1 (10 μm/10 μm). At V_g=−12 V, the MESFET is almost pinched off. The solid symbols in Fig. 3 represent the saturation points (V_{dsat}, I_{dsat}) and they were selected at the point where the increase of I_{ds} with V_{ds} starts to become negligible (~1×10^{-7} A). The saturation points at different gate voltages follow an empirical relationship,

$$I_{dsat} = I_{dsat|V_g=0}(V_{dsat}/V_P)^2, \tag{1}$$

where V_P is the pinch-off voltage determined by the channel doping concentration N_D and the channel thickness a as $V_P = qN_Da^2/2\varepsilon_s$. The V_P measured in Fig. 3 by fitting $I_{dsat} \sim V_{dsat}$ to Eq. (1) is 15 V, consistent with the value calculated from the V_P equation using a channel doping concentration of 1×10^{17} cm^{-3} and channel thickness of ~0.4 μm.

From Fig. 3, the maximum transconductance and channel conductance were calculated to be ~30 μA/V for the channel width/length ratio of 1:1, which is two or three times better than the previously reported results.[3] The improvement is likely due to better quality of the GaP epilayer grown by MBE and lower contact resistance. The transconductance g_m can be calculated from

$$g_m = aq\mu_n N_D\left(\frac{W}{L}\right)\left(1 - \sqrt{\frac{\psi_0 - V_g}{V_P}}\right), \tag{2}$$

where ψ_0 is the Schottky barrier height for MESFET or *p-n* junction barrier for JFET. Maximum g_m is reached near V_g=0 V. The prefactor in Eq. (2), $aq\mu_n N_D$ (W/L), represents

an ideal transconductance which can be estimated to be $\sim 96\ \mu A/V$ in our devices, using the bulk electron mobility of $\sim 150\ cm^2/V\ s$ for GaP. Based on $\psi_0 \sim 1.1$ V for Cr–GaP junction and $V_P \sim 15$ V, a maximum $g_m \sim 70\ \mu A/V$ is expected on GaP MESFETs. The discrepancy between measurement and theory is caused by lower carrier mobility and series resistance R_s in actual devices. Using the assumed bulk electron mobility of $\sim 150\ cm^2/V\ s$, R_s can be calculated to be $10-20\ k\Omega$. This simple calculation cannot separate contact resistance and material sheet resistance, both of which contribute to R_s. Such a high series resistance could significantly lower g_m; therefore, improved transconductance is expected on transistors with low-R_s contacts, e.g., ion-implanted contacts. It should be noted that the calculated R_s might be overestimated, since the actual channel mobility is likely to be lower than the bulk mobility that was used in the calculation. The transconductance of GaP FETs is relatively low compared to that of Si and GaAs FETs, due to the significantly lower mobility of GaP. Therefore, the niche market of GaP devices exists in low-noise applications that utilize its wide band gap but not in high-frequency applications requiring high mobility. In addition, the channel width/length ratio of GaP FETs may be appropriately designed to provide higher transconductance and channel conductance to a certain degree.

In summary, FETs play an important role in the niche applications of GaP circuits. The fabrication details and measured characteristics of MESFET and JFET on MBE GaP are reported in this letter. The electrical characteristics can be used to estimate GaP material properties and to discuss the transistor performance limitations. Future optimization of the transistor performance relies on improving the carrier mobility in GaP epilayer and minimizing parasitic resistances in actual devices.

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