Demonstration of npn InAs Bipolar Transistors with Inverted Base Doping

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***Abstract*—We demonstrate np^+n InAs bipolar transistors that operate under room temperature and cryogenic conditions. InAs transistors on an InP substrate were characterized as a function of temperature and exhibited good room temperature and low temperature common-emitter characteristics. Although the base doping density exceeded the emitter doping density by a factor of 20, current gains of 30 were achieved at room temperature. Junction leakage currents and contact resistance were identified as problems to address.**

I. Introduction

OHTA has presented a scaling principle for bipolar transistors that involves downscaling the operating temperature and semiconductor bandgap as the transistor dimensions are reduced [1]. The result would be a high-speed but low-power bipolar technology well-suited to cryogenic applications, including interfacing to superconducting or quantum effect devices. InAs is a promising semiconductor for such applications because of its appropriately small bandgap (E_G = 0.36 eV at 300K) and excellent transport properties. Several groups have investigated InAs as the channel region for heterostructure field-effect transistors (HFETs) and for resonant tunneling structures [2]–[5], and Pnp InAs-based HBTs have been reported [6]. Compatible heterojunctions produce large conduction band discontinuities which have, however, thwarted the development of Npn InAs-based HBTs [7]. In this letter, we report the demonstration of npn InAs bipolar transistors.

To circumvent the lack of a compatible wide-bandgap emitter for Npn HBTs, we explored all-InAs pseudo-HBTs, where effective bandgap narrowing in a heavily doped base is expected to produce a pseudo-heterojunction at the emitter-base interface [8], [9]. The effectiveness of this approach has been demonstrated for Si [9] and GaAs pseudo-HBTs [10]. Similar effects are expected in InAs, and degeneracy effects, which widen the effective bandgap in the emitter [11], should be even stronger. InAs should, therefore, lend itself well to the construction of Npn pseudo-HBTs.

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II. Experimental Results and Discussion

The InAs pseudo-HBT structure shown in Fig. 1 was grown by molecular beam epitaxy in a Varian GEN-II system. The film was grown lattice-mismatched on an InP substrate, opening the possibility of high-frequency operation with good device isolation and low parasitic capacitance by using semi-insulating InP substrates. (For ease of processing, however, the present structure was grown on a conducting substrate). An InGaAs layer, lattice-matched to InP, was grown on the n^+ substrate, followed by a 0.5 μm region over which the composition was graded to pure InAs and a 1.0 μm heavily-doped n^+ InAs subcollector. The p^+ base was Be-doped to 1×10^{19} cm^{-3}. A 700 Å thick intrinsic layer was grown between the base and the emitter to reduce tunneling currents, which become important at low temperature [10]. Secondary ion mass spectroscopy of a similar film showed good dopant calibration. Transistors were fabricated using a simple non-self-aligned process and wet chemical etching using a 4 H_3PO_4 : 1 H_2O_2 : 50 H_2O solution. Emitter and base contacts were electron-beam evaporated Ti/Au.

Packaged devices were tested in a closed-cycle cryostat. The base-emitter junctions exhibited good reverse-bias characteristics, with little leakage current, indicating the success of the intrinsic spacer layer. The base-collector junctions displayed more leakage and lower breakdown voltages than the base-emitter junctions. This may be due to the absence of a spacer layer in the base-collector junction, but may also indicate dislocations in this lattice-mismatched film. Large devices showed emitter-collector short circuits, which we attribute to threading dislocations. As the temperature was lowered, the reverse-leakage current reduced and the breakdown voltage increased.

Transistor operation was confirmed, with 24×24 μm^2 transistors displaying a room temperature current gain of 30 at a current density of 1.5×10^4 A/cm^2. Larger devices (80×80 μm^2 and above) show high collector leakage currents in their common-emitter characteristics, but smaller devices possess good common-emitter characteristics, as shown in Fig. 2 for a 24×24 μm^2 device at room temperature. Even for these smaller devices, however, the room temperature breakdown voltage was less than 0.5 V, because of the

n InAs	$5x10^{18}$ cm^{-3}	500 Å
n InAs	$5x10^{17}$ cm^{-3}	3000 Å
i InAs		700 Å
p InAs	$1x10^{19}$ cm^{-3}	1000 Å
n InAs	$1x10^{16}$ cm^{-3}	0.6 μm
n InAs	$1x10^{18}$ cm^{-3}	1.0 μm
grade to InAs	$2x10^{18}$ cm^{-3}	0.5 μm
n $In_{0.6}Ga_{0.4}As$	$2x10^{18}$ cm^{-3}	0.5 μm
n^+ InP	substrate	

Fig. 1. InAs film structure.

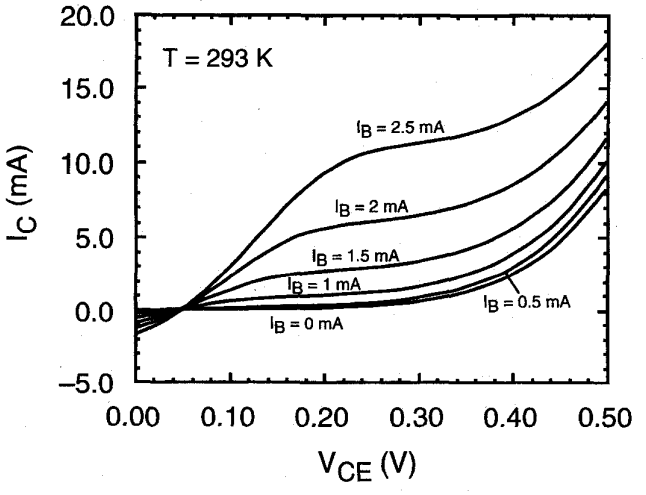

Fig. 2. InAs transistor common-emitter characteristics at room temperature. Base currents are 0 to 2.5 mA in 0.5 mA steps and the emitter size is 24 × 24 μm^2.

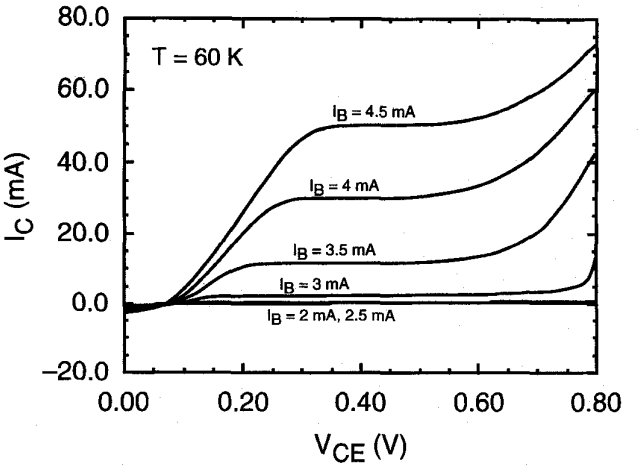

Fig. 3. InAs transistor common-emitter characteristics at 60 K. The base currents are 2 mA to 4.5 mA in 0.5 mA steps, and the device size is 24 × 24 μm^2.

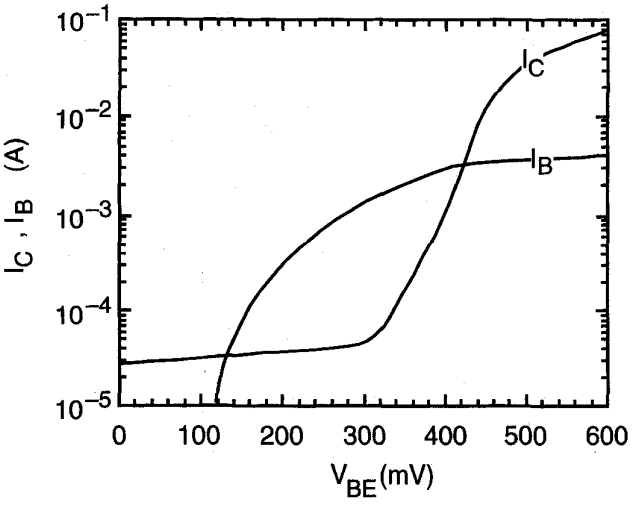

Fig. 4. Gummel plot of 24 × 24 μm^2 InAs transistor at T = 30 K. The base-collector junction reverse bias is 150 mV.

low reverse-bias breakdown of the base-collector junction. As the transistors were cooled, their characteristics improved significantly, with collector breakdown voltages BV_{CEO} approaching 1V at 100 K. The common-emitter characteristic of the same transistor shown in Fig. 2 is displayed in Fig. 3 for operation at 60 K. The much improved output resistance is easily observed as collector reverse-leakage is reduced at low temperature.

For a transistor with a wide gap emitter, the gain should increase as the temperature is lowered, *if* the base current is dominated by back-injection of holes into the emitter. We found, instead, that the current gain dropped somewhat as the temperature was lowered, from 30 at room temperature to just over 20 at 30 K. This behavior could be the result of excess base-emitter leakage, which is relatively temperature insensitive. This leakage current is clearly seen in Fig. 4, a 30 K Gummel plot of the same 24 × 24 μm^2 transistor shown in Figs. 2 and 3. A similar film, but grown lattice-matched on an InAs substrate, showed much better Gummel characteristics (the common emitter characteristics, however, suffered from a high series resistance). For the device on the InAs substrate, the room temperature ideality factors were $n \approx 1$ for the collector current and $n \approx 2$ for the base current. As the temperature was lowered, the base current ideality factor steadily increased to $n \approx 10$ at 77 K. (Below room temperature, the combined effects of leakage and series resistance made it impossible to identify an ideality factor for the collector current.) The non-ideal base current appears to dominate hole back-injection leading to a reduction of β at low temperatures. The source of the excess base leakage current and the reason for the increase in the lattice mismatched film have not been identified. Dislocations in the lattice mismatched films may play a role as may n-type surface channels on the exposed p-type base, which could result from Fermi level pinning in the conduction band [12]. The characteristics are

also consistent with defect-assisted tunneling through a space-charge layer [13].

The motivation for this work was to demonstrate that effective bandgap narrowing could be utilized in InAs to realize Npn pseudo-HBT operation without the use of a true wide bandgap emitter. The results are not conclusive because they are clouded by extraneous leakage currents. One could achieve a current gain of 30 in an ideal transistor without effective bandgap narrowing, if $\mu_n/\mu_p \approx 200$. In our devices, however, β increases monotonically with I_c, which clearly indicates that the gain is not limited by back-injected holes. The back-injection-limited current gain must, therefore, be substantially greater than 30, which would require a still higher mobility ratio. It does not seem possible to explain such large values with reasonable estimates of the electron and hole mobilities unless effective bandgap narrowing is postulated. Nevertheless, a clear picture of pseudo-HBT operation in these structures must await the identification and suppression of junction leakage currents.

III. Summary

InAs np^+n bipolar transistors were fabricated and characterized under room and low-temperature operation. Current gains of 30 were achieved, despite the fact that the base doping density was 20 times the emitter doping density. At low temperatures, devices displayed a highly non-ideal base current characteristic and showed the effects of parasitic resistances. If these issues can be successfully addressed, InAs npn bipolar transistors may prove useful in high-speed, low-power cryogenic applications.

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