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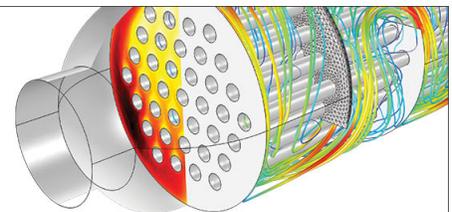
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Evidence for misfit dislocation-related carrier accumulation at the InAs/GaP heterointerface

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The electrical properties of the mismatched interface between InAs and GaP have been investigated. High-resolution transmission electron microscopy images show the presence of strain relieving, 90° misfit dislocations at this interface. Hall measurements and electrochemical capacitance–voltage profiling indicate the presence of a high-density sheet of carriers (electrons and holes) at the interface. A linkage is drawn between interfacial carriers and misfit dislocations. A model based on Fermi-level pinning in InAs at the interface by misfit dislocations is proposed to account for the observed electrical behavior. © 1998 American Institute of Physics. [S0003-6951(98)04016-9]

The growth of epitaxial layers on lattice-mismatched substrates is a topic that has attracted considerable research interest. The modes of epilayer growth and the associated strain relief through the formation of interfacial misfit dislocations have been studied for a variety of semiconductor systems. Most of the attention has been focused on avoiding high interfacial and threading dislocation densities, as these defects are known to adversely affect device performance.^{1,2} Comparatively few studies have been carried out on the electrical activity of misfit dislocations in III–V heteroepitaxial systems. Similarly, electrical properties of mismatched interfaces have not been well characterized.

In the present study, we have investigated the direct growth of InAs on (001) GaP substrates. This system displays unique properties due to the high mismatch in lattice parameter (11%) as well as the large difference in band gap (InAs: 0.36 eV; GaP: 2.26 eV). The strain due to lattice mismatch is relieved by the formation of a regularly spaced (~4 nm) array of (predominantly) 90° pure-edge misfit dislocations at the InAs/GaP interface.³ The large band offset between InAs and GaP creates a large confining potential at the interface, which ensures that the heterojunction is depleted of carriers.

InAs was grown on (001) GaP by solid-source molecular beam epitaxy (MBE) using a Varian GEN-II MBE system. Commercially obtained (001) GaP substrates were thermally cleaned in the growth chamber under a P_2 over pressure. A 100 nm GaP buffer layer was grown followed by the growth of a 20 period superlattice consisting of 5 nm alternating layers of GaP and AlP in order to prevent the outdiffusion of sulfur from the substrate. Finally, a 200 nm buffer layer of p -GaP ($3 \times 10^{16} \text{ cm}^{-3}$) was grown.

An undoped InAs epilayer was grown at 350 °C. The first few monolayers of InAs were grown under low V/III beam flux ratios to promote a smoother interface. Reflection high-energy electron diffraction was used to monitor surface

morphology and growth rates during the deposition. Finally, a 5 nm capping layer of undoped $\text{In}_{0.8}\text{Al}_{0.2}\text{As}$ was grown above the InAs layer. Samples with varying thickness of InAs in the range of 5–30 nm were grown in this manner.

The electrical behavior of the InAs layer and the InAs/GaP heterointerface was examined, with emphasis on understanding electrical activity of the misfit dislocations at the interface. Lateral conductivity and depth carrier profiling were employed to characterize the InAs layer. The interface structure was investigated using high-resolution cross-sectional transmission electron microscopy (HRTEM). A model based on Fermi-level pinning at the interface by misfit dislocations is postulated to explain our observations.

Cross-sectional TEM studies were performed using a JEOL 2000 FX microscope with a beam energy of 200 keV. The samples examined maintained an epitaxial relationship between InAs and GaP in all cases. Figure 1 shows a HRTEM micrograph of the InAs/GaP heterointerface. A regularly spaced array of predominantly 90° misfit dislocations oriented along $\langle 110 \rangle$ direction is clearly visible at the interface. The portions of the interface between the dislocations appears to be atomically smooth and free of distortions. Thus, HRTEM shows that the main structural defects at the interface are 90° misfit dislocations.

Hall-effect measurements were performed at room tem-

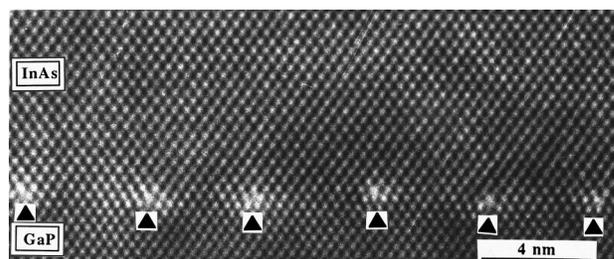


FIG. 1. HRTEM micrograph of an InAs epilayer grown on GaP displaying an interface with a regularly spaced array of 90° misfit dislocations (arrowed).

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TABLE I. Sheet carrier concentration and Hall mobility data for InAs epilayers of varying thickness grown on GaP at room temperature and liquid-nitrogen temperature.

Sample No.	InAs Thickness (nm)	Room temperature		77 K	
		Sheet density (cm^{-2})	Hall mobility ($\text{cm}^2/\text{V s}$)	Sheet density (cm^{-2})	Hall mobility ($\text{cm}^2/\text{V s}$)
1	5	1.5×10^{13}	40	1.5×10^{13}	25
2	10	1.2×10^{13}	500	1.0×10^{13}	360
3	15	0.75×10^{13}	335	0.75×10^{13}	310
4	20	1.0×10^{13}	460	0.9×10^{13}	430
5	30	0.7×10^{13}	795	0.6×10^{13}	730

perature and at 77 K using both a Hall bar and a standard van der Pauw geometry. The Hall bars were transferred by photolithography on the samples, followed by a Ti/Au metallization and mesa etching. For the van der Pauw measurements, approximately square specimens were cleaved and In dots were alloyed at the four corners at 300 °C in an inert gas atmosphere. The sign of the Hall coefficient for each of the samples tested indicated that the majority carriers were electrons. Table I lists the Hall mobility and sheet carrier concentrations for samples of differing InAs thickness. It is noteworthy that the sheet carrier density was very high ($\sim 10^{13} \text{ cm}^{-2}$) and did not vary as a function of epilayer thickness. This is indicative of a localized high-density sheet of electronic charge in our samples. No “freeze-out” of carriers at liquid-N₂ temperature was observed. However, a slight decrease in Hall mobility at 77 K was observed.

Carrier-concentration depth profiling was carried out on a sample with 12.5 nm InAs and a 0.4 μm capping In_{0.8}Al_{0.2}As layer in order to understand the distribution of carriers. This was performed using an electrochemical capacitance voltage profiler manufactured by Bio-Rad Micromeasurements, Inc. A depth resolution of 1 nm can be achieved with this profiler.⁴ The resultant semilog plot of carrier concentration versus depth is shown in Fig. 2. A spike in the carrier concentration at the InAs/GaP heterointerface is clearly evident. This sharp increase in carrier concentration occurs over a very narrow region of ~ 1 –2 nm, thus confirming the presence of a high-density sheet of charge localized at the interface.

We propose an explanation of these results on the basis

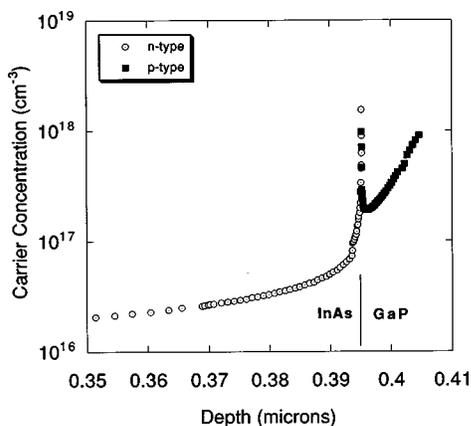


FIG. 2. Electrochemical capacitance-voltage profile of carrier concentration vs depth for the (undoped) InAs/(p)GaP heterostructure.

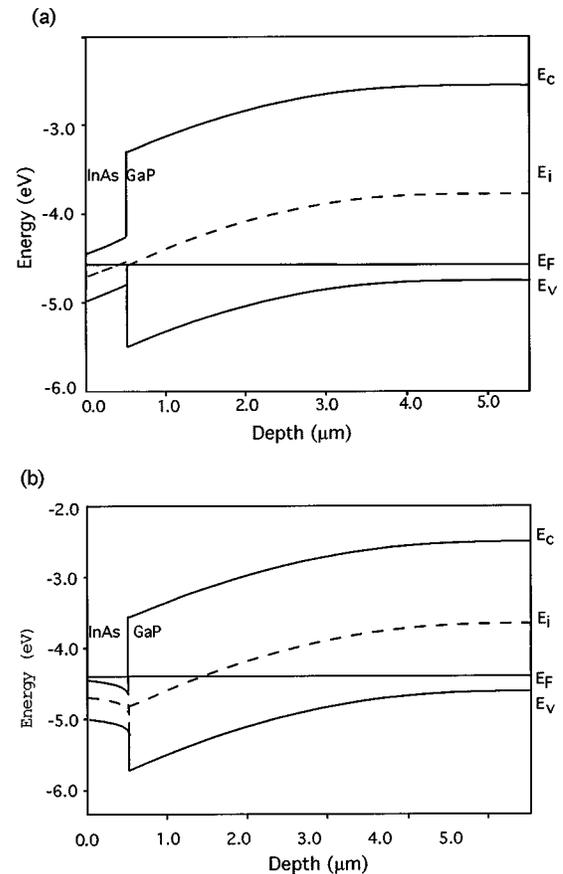


FIG. 3. (a) ADEPT simulation of an “ideal” InAs/GaP heterostructure. (b) ADEPT simulation of the InAs/GaP heterostructure with a sheet of electronic charge at the interface. Note that the Fermi level is pinned in the conduction band at the interface.

of the following simple model. A linkage is drawn between the existence of sheet charge and the presence of misfit dislocations at the heterointerface. Carrier generation apparently occurs in this system at the heterointerface. The most likely agent for generation is the network of misfit dislocations. Free surfaces and defects are known to pin the Fermi level in the conduction band in InAs, thus making the semiconductor degenerate.^{5,6} Here, the misfit dislocations are proposed to pin the Fermi level at the interface in the conduction band, and thus, give rise to a sheet of electronic charge.

To test these hypotheses in terms of an energy-band model, simulations of InAs/GaP were created using the simulator ADEPT. Figure 3(a) shows the simulated band diagram for the “ideal” n^- -InAs/ p^- -GaP interface. Undoped InAs, being a narrow-gap semiconductor, is expected to be n^- due to thermal carrier generation. The Fermi level of the InAs at the interface is seen to be at midgap. The band bending displayed here indicates that the interface must be depleted of charge and rectifying in nature. Figure 3(b) shows the simulated band diagram with a high-density (10^{13} cm^{-2}) sheet of electrons inserted at the interface. The Fermi level at the interface is now pinned 0.2 eV above the conduction-band edge and the band diagram shows a narrow potential well in the InAs, which can act as a two-dimensional electron gas (2DEG) confining carriers near the interface.

Thus, it appears that the effect of the array of misfit dislocations is to generate electrons, which are then confined in a 2DEG near the interface. These carriers would be ex-

pected to be strongly scattered by the dislocation network, which results in the low mobility values. As the temperature is decreased, the confinement of the carriers would be even stronger, i.e., the mobility would decrease with decreasing temperature, the opposite of the normally expected μ - T relationship. This is consistent with the observations made of this system. Ideal electron mobility in InAs is $33\,000\text{ cm}^2/\text{V s}$.⁷ As seen from Table I, however, the measured mobilities are only a small fraction of the ideal value, indicating strong carrier scattering. Further, the mobilities fall slightly at lower temperature, as expected in this model.

From the results and discussion presented here, it is apparent that the InAs/GaP system has unique interfacial properties, which holds promise in device applications. In particular, the misfit dislocations could act as conducting channels for the carriers, akin to the presence of a 2D network of “metallic” wires in a more resistive medium.

To conclude, we have demonstrated the existence of a high-density sheet of electrons at the InAs/GaP heterointerface. A linkage may exist between this sheet of charge and the interfacial misfit dislocations. A simple model to explain carrier generation by misfit dislocations has been proposed, which is consistent with the observed conduction behavior.

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