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Photo-Enhanced Etching of *n*-Si

H. J. Hoffmann* and J. M. Woodall

IBM-Thomas J. Watson Research Center, Yorktown Heights, New York 10598, NY, USA

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Abstract. The etch rate of *n*-type Si in diluted HF solutions was investigated as a function of the bias voltage applied to the Si/electrolyte interface in the dark and under illumination. It was observed that the etch rate depends very sensitively on the minority carrier flow through this interface. For an illumination intensity of 5.3×10^{16} photons/cm^2 s ($\lambda = 550$ nm) and the depleted Si/electrolyte interface biased slightly (less than 1 V) in reverse, the etch rate is increased by a factor of more than 1000 as compared to the etch rate under open-circuit condition. This effect can be used to create etch patterns during device processing without prior masking the semiconductors. Using the same effect it should be possible to trim the thickness of Si layers on (semi-) insulating substrates for the fabrication of enhancement-mode FETs.

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Etching solutions for semiconductors consist usually of an oxident and a complexing agent which causes the dissolution of the oxidized semiconductor surface (see e.g. [1]). For Si the oxident is very often nitric acid (HNO_3) and the complexing agent is usually fluoric acid (HF). Without oxident the etch rate is considerably reduced. The etch rate of the (111) surface of *n*-Si, e.g., is in the range between 15–1700 μm/min depending on the HF : HNO_3 ratio [2], whereas it is as low as 0.3 Å/min at 25 °C in 48% HF solution alone [3, 4]. Hu and Kerr [4] reported slightly larger values than 0.3 Å/min after diluting the HF solution and adding $NaC_2H_3O_2$ or NaF. But even then, the etch rate does not exceed 0.78 Å/min. These authors observed also that these low etch rates were independent of the O_2 content of the etching solution.

In contrast to this, however, we report in the following on a series of experiments that show how one can increase the etch rate of HF solutions considerably by using light in lieu of an oxident. We tested how and under what conditions the etch rate of Si can be controlled by the illumination, since the availability of a light-controlled etch rate has several promising consequences for device processing applications as we will discuss subsequently.

* Present address: Schott Glaswerke, Hattenbergstrasse 10, D-6500 Mainz, Fed. Rep. Germany

For the etching experiments we used (111) surfaces of prepolished *n*-type Si wafers with $0.3–0.8 \times 10^{15}$ cm^{-3} charge carriers. After providing the back sides of the samples with ohmic In contacts, we connected them with silver paste to the electrode of a sampleholder. Thereafter the samples were partly covered with black wax in order that only the uncovered surface could be attacked by the etching solution. The area of the uncovered Si surface varied between 4 and 25 mm^2. This surface was the working electrode in a three-electrode electrochemical cell. A saturated calomel electrode (SCE) was the reference electrode and a 4 cm^2 platinum sheet the auxiliary electrode. The electrolyte consisted of 1 part HF (48%) diluted in 9 to 19 parts deionized water. The temperature was 24 ± 3 °C. The *n*-Si/electrolyte interface was either kept in the dark or illuminated through an interference filter with a transmission maximum at a wavelength of 550 nm and a full width at half maximum of 25 nm. The penetration depth into Si for light with this range of wavelength is about 1.5 μm.

Figure 1 shows the I–V characteristics of the *n*-Si/electrolyte interface without (Fig. 1a) and with illumination (Fig. 1b) for a small interval of voltages. For zero current there is a voltage of −0.37 V between the sample and SCE in the dark and −0.55 V under illumination with 5.3×10^{16} photons/cm^2 s. The open-

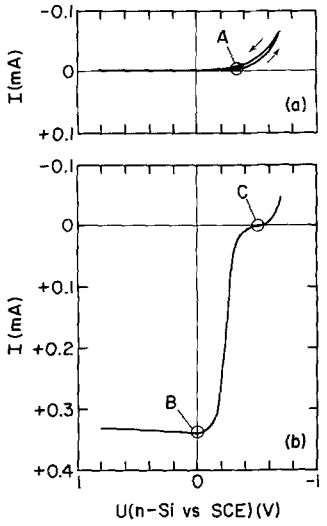

Fig. 1a and b. I–V characteristics of the *n*-Si/HF solution contact in the dark (a) and under illumination (b). The sweep rate of the voltage is 40 mV/s

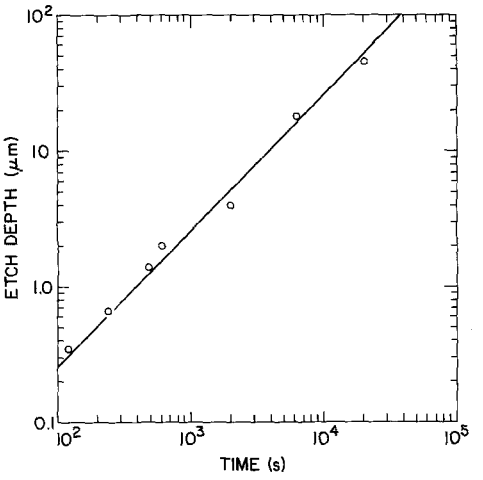

Fig. 2. Etch depth as a function of time for working point B of Fig. 1b

circuit photovoltage of −0.18 V is rather small for this illumination intensity because of the formation of a thin oxid layer on the Si surface. The interference colors due to this layer could clearly be observed. Furthermore, due to electric charges in the oxid layers the I–V characteristics could shift horizontally by several tenths of a Volt to higher voltages. The shape of the I–V characteristics, however, remained nearly unchanged.

In order to avoid too large anodic currents in the dark, the bias voltages for the etching were chosen within the range of voltages given by the I–V characteristic in Fig. 1. Due to these undesired currents at larger anodic voltages [1], the sample would be decomposed even in the dark and the etching would not be controlled by the illumination. Among the large variety of different bias and illumination conditions we consider the following three typical cases, only.

At working point A in Fig. 1a, there is no illumination and no external bias voltage applied to the *n*-Si/electrolyte contact. These conditions result in the very low etch rates which are already known from [3, 4].

For working point C in Fig. 1b, the interface is illuminated; the *n*-Si/electrolyte contact, however, is kept still under open-circuit conditions, i.e. there is no external voltage applied to the electrochemical cell and no external current. This results in an etch rate of $(2 \pm 1) \times 10^{-2}$ Å/s for our illumination level. With the semiconductor/electrolyte contact biased externally in reverse direction we shifted the working point from C to B. The etch rate increased proportional to the reverse photocurrent. The etch depth as a function of time at working point B is shown in Fig. 2. From the figure we obtain an etch rate of 26 ± 7 Å/s. This value is larger than the etch rate at working point C by a factor of approximately 1000. This large difference between the etch rates at working points B and C can be understood as follows: Removing electrons from or adding holes to the Si surface is equivalent to oxidation of the surface atoms. Since the holes are created by the illumination not only on the surface (as is done by chemical oxidants) but also in a layer reaching into the bulk, the flow of minority carriers towards the Si surface can be controlled by a bias voltage. At working point C most holes which are generated by the illumination recombine with electrons before they can reach the semiconductor/electrolyte interface. Only a small fraction of holes (in our case less than 0.1%) reach that interface. This results in a slight increase of the etch rate at working point C as compared to that of working point A. With increasing reverse bias voltage, however, the hole current towards the Si/electrolyte interface and thus the etch rate increase by several orders of magnitude until it saturates when nearly all photo-holes reach that interface. Then the etch rate due to the illumination is maximum. Assuming that 2 holes are needed in order that a Si atom at the surface can be dissolved at low anodic voltages [5–10], we calculate a quantum efficiency of nearly 50% for the photoetching at working point B, not correcting for the reflection losses at the semiconductor/electrolyte interface and at the optical window of the electrochemical cell.

The possibility to control the etch rate of *n*-Si over quite a large interval by the illumination intensity and the applied bias voltage has several promising consequences with respect to device processing applications.

The photoetching effect can be applied to create etch patterns without prior masking, only by optical imaging the desired masks and applying a small reverse bias voltage during the etching process. This can replace, e.g., the usually awkward masking with negative and positive photoresist. Thus the fabrication of microelectronic structures on Si wafers can be simplified considerably. Furthermore, one can create profiles with *variable* depth very easily in the wafers since the etch rate can be varied locally with the light intensity. This is an additional degree of freedom for the design of microelectronic devices. The lateral resolving power of the etching process is limited either by the diffusion length of the holes or by the resolving power of the illumination system to create the etch profile. If it is limited by the diffusion length, the present photoetching process can be used to determine the diffusion length of the holes in the samples simply by measuring the broadening of suitable test patterns. This may be a quite convenient method to measure this material parameter, because the test patterns have to be imaged by an optical system, only, on the semiconductor/electrolyte interface.

Since the etch rate is controlled by the flow of holes to that interface, the present photoetching is furthermore expected to be self-limited if the thickness d of Si layers on (semi-)insulating substrates becomes smaller than the initial depletion layer depth l. The mechanism for this self-limitation is the same as that described in a former paper for GaAs [11]: As long as the thickness d of the Si layer is larger than l, nearly all minority carriers created by the illumination can reach the Si/electrolyte interface under a small reverse bias voltage (working point B in Fig. 1b). If, however, d is equal or even smaller than the initial depletion layer depth l, the semiconducting layer is pinched off. Thus the electrical conductivity under that contact area is reduced. Since, in addition, the band bending becomes smaller with decreasing d, the working point of the photoetching is shifted automatically from B to C, i.e. the etching process is slowed down considerably. Thus one can use the photoetching effect to trim automatically the thickness of Si layers during the fabrication of normally-off FETs.

Until now, we tested the present procedure with crystalline Si and GaAs. We believe that the same technique can be applied also to amorphous Si and SOS structures. Other semiconducting materials can be taken into consideration, too, if suitable complexing agents and solvents are used.

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