A rough estimate for the sputtering yield was obtained from the time it took to etch through the silicon target. After the measurements at different fluxes and temperatures we could calculate a mean etch rate of 2500 Å/min corresponding with a sputtering yield of roughly 15 Si atoms per incoming Ar^+ ion.

In conclusion, we can say that ion-assisted etching by means of physisorbed SF_6 on Si is quite efficient. The etch rate is in between that for XeF_2 and Cl_2. Clearly dissociation of SF_6 and breaking of Si–Si bonds by the ion bombardment leads to new chemical products like SiF_x with $x \leqslant 4$. Sputtering of species SiF_x with $x < 4$ is similar to sputtering of the chlorine compounds in the case of chlorine-assisted etching[3,5] and shows a collision cascade behavior. The energies of SiF_4 itself are about an order of magnitude lower. Like in the case of chlorine-assisted etching we can assume that the fluorides are present in the amorphized silicon matrix since their presence on the surface would undoubtedly have given rise to evaporation.[15]

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Controlled low barrier height n^+-InGaAs/n-GaAs pseudomorphic heterojunction Schottky diodes

A. W. Kleinsasser, J. M. Woodall, G. D. Pettit, T. N. Jackson, J. Y.-F. Tang, and
P. D. Kirchner
IBM T. J. Watson Research Center, P. O. Box 218, Yorktown Heights, New York 10598

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Heterojunction Schottky barrier diodes, in which a pseudomorphic layer of n^+-InGaAs played the role of a metal contacting n-GaAs, were grown by molecular beam epitaxy. The junctions had low barrier heights (30–150 meV) which could be controlled by composition and doping of the n^+ layer. I-V measurements of the devices confirmed that the devices behaved as Schottky diodes, in accordance with the theory of tunneling and thermally assisted tunneling in the temperature range 4–200 K. An exponential increase in conductance with decreasing In concentration indicates a decrease in barrier height which is at least qualitatively consistent with simulations of the barriers based on earlier experiments, which showed that the band-gap discontinuity appears predominately in the conduction band.

Metal-III-V compound semiconductor interfaces exhibit Fermi level pinning, resulting in Schottky barrier heights which can be varied over only a relatively small range.[1,2] A number of models attempt to explain this behavior; however, at the present time none has sufficient precision to aid in the development of contacts suitable for field-effect transistor (FET) devices in large scale integration (LSI) applications. In the case of GaAs, for example, the two major contact problems are (1) a gate Schottky barrier of about (but not exactly) 0.8 eV and (2) a source and drain ohmic contact metallurgy (Au-Ge-Ni) which is unstable to subsequent processing above 400–500 °C highly dependent on subtle processing conditions, and not understood theoretically.[3] Recent laboratory successes notwithstanding, it is quite possible that the variability in Schottky barrier heights and contact resistances in current technology could limit the usefulness of GaAs in LSI applications. In addition it is not possible, with known metal-semiconductor contacts, to arbitrarily control barrier heights in order to fabricate devices which are optimized for low-temperature applications in which low barriers are needed.

In carefully prepared lattice-matched isoelectronic heterojunctions (e.g., GaAlAs/GaAs) Fermi level pinning is absent, the height and shape of the interfacial barrier are determined by band alignment and doping. This property is used in such devices as double heterostructure (DH) lasers and high electron mobility transistors. However, except for an early report by Chandra and Eastman[4] on GaAs/GaAlAs *n-n* heterojunctions, structures which utilize majority-carrier transport normal to the interface (e.g., Schottky barrier diodes) have not been widely studied. However, modern epitaxial growth techniques such as molecular beam epitaxy (MBE) and metalorganic chemical vapor deposition (MOCVD), which permit good control of layer thickness, doping, and composition, should allow fabrication of such structures with sufficient control of the barriers to meet device requirements. We report here the first results on the fabrication and characterization of MBE-grown *n*-InGaAs–*n*-GaAs heterojunction Schottky diodes with low barriers (30–150 meV), in which the barrier height is controlled by band offset and doping level rather than by Fermi level pinning.

Although the lineup of the bands at heterojunction interfaces is not well understood,[5–7] in many cases (such as InGaAs/GaAs most of the band-gap discontinuity is taken up by the conduction band,[7] giving the possibility of major-carrier devices based on controllable barriers to electron transport (e.g., *n-n* isotype heterojunction diodes). The conduction-band shape at interfaces between 1×10^{18} *n*-$\mathrm{In}_x\mathrm{Ga}_{1-x}\mathrm{As}$ ($x = 0.07, 0.10, 0.15$) and 2×10^{16} *n*-GaAs is illustrated in Fig. 1. This plot was obtained by solving Poisson's equation for the InGaAs/GaAs heterojunction system using MONTE, a general device simulator[8] which incorporates Fermi-Dirac statistics for the electron gas and uses a finite difference scheme. A conduction-band discontinuity of 85% of the band-gap difference, which is a known function of composition,[9] was assumed. The structure forms a Schottky barrier diode in which the InGaAs plays the role of the metal. The barrier height E_B is approximated by $E_B \simeq \Delta E_c - \xi_2$, where ΔE_c is the total conduction-band offset at the interface and ξ_2 is the Fermi level degeneracy in the InGaAs layer (the exact result includes the small band bending in the InGaAs and ξ_1, the Fermi level degeneracy in the GaAs). Thus the diode barrier height is determined primarily by the composition and doping of the InGaAs layer, and is adjustable over a wide range. For a given height, the depletion width (barrier shape) is determined by the doping in the GaAs layer.

The structures used in these experiments consisted of semiconductor multilayers, grown by MBE on conducting GaAs substrates. Care was taken to ensure that the InGaAs layer was thin enough to be pseudomorphic, i.e., that no misfit dislocations were formed at the InGaAs/GaAs interface. The composition of the InGaAs layer was graded back to GaAs. Early attempts to grade this layer to pure InAs to aid in ohmic contact formation resulted in misfit dislocation formation at the critical InGaAs/GaAs interface (it is known[10] that misfit dislocations are electrically active and will pin the Fermi level, negating the effects of the band offsets). Junction area was defined by chemical etching, which was terminated above the epi-substrate interface in order to avoid any deleterious effects such as Fermi level pinning at that interface. Low resistance Au-Ge-Ni ohmic contacts were made to the structures and to the back of the wafer (contact resistance was always much lower than the junction resistance). Alloying was done carefully, so that the contact did not penetrate into the active region of the junctions.

Electron transport in these structures is due to thermionic emission (TE) over or tunneling through the barrier. Tunneling or field emission (FE) dominates at low temperatures (in which the electrons have insufficient energy to surmount the barrier). Field emission is large in samples with heavy doping and/or low barrier height. Due to the decrease in barrier width with increasing energy, the energy distribution of tunneling electrons can be rather narrowly peaked at an energy between the Fermi level and the top of the barrier at intermediate temperatures, giving rise to a well-characterized regime of temperature–assisted tunneling, or thermionic field emission (*T*-FE).[11,12] Current-voltage characteristics are ohmic (linear) for low biases ($J = V/R_0$), and exponential for large biases ($J = J_s e^{qV/E}$). The parameters R_0, J_s, and E_0, and their dependence on temperature, contain information on the barrier, including the barrier height, and indicate the crossover between the various conduction

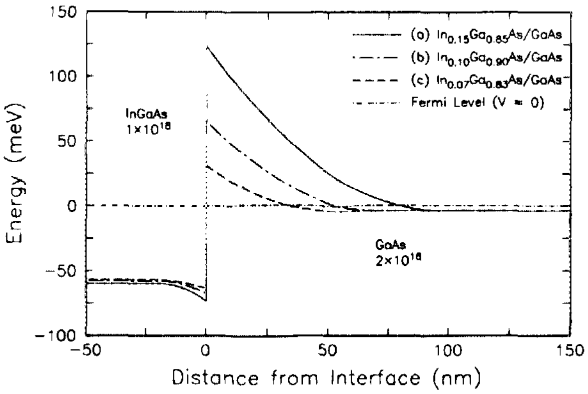

FIG. 1. Behavior of the conduction band near the *n*-$\mathrm{In}_x\mathrm{Ga}_{1-x}\mathrm{As}$/*n*-GaAs heterojunction interface, in absence of applied bias, for the three samples described in the text: (a) $x = 0.15$ ($\Delta E_c = 198$ meV, $E_B = 125$ meV, and $w = 96$ nm), (b) $x = 0.10$ ($\Delta E_c = 134$ meV, $E_B = 67$ meV, and $w = 71$ nm), and (c) $x = 0.07$ ($\Delta E_c = 95$ meV, $E_B = 31$ meV, and $w = 51$ nm). In all three, $\xi_1 = 4$ meV ($N_D = 2\times10^{16}$), $\xi_2 = 57$ meV ($N_D = 1\times10^{18}$), and $T = 10$ K.

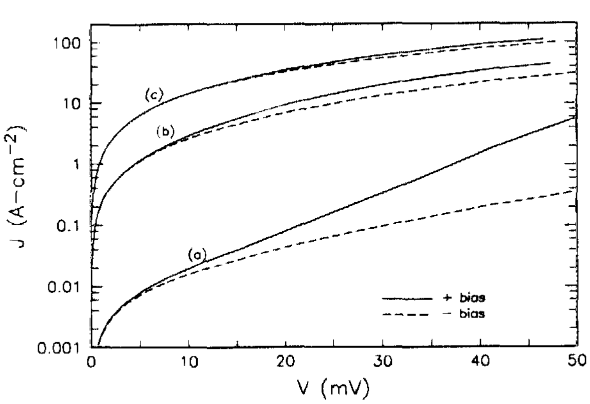

FIG. 2. Semilog plot of the current-voltage characteristics of the three devices described in Fig. 1. Absolute values of both foreward and reverse characteristics are shown. Note that only the composition of the InGaAs layer was varied between the three samples; this plot thus illustrates the exponential increase in the conductance of these structures as the barrier height is lowered by reducing the In concentration.

regimes. At low temperatures, E_0 has the value $E_{00} = (qh/4\pi)(N_D/\epsilon m)^{1/2}$, which is a characteristic energy for tunneling.[2,11,12] The three regimes of conduction are defined by $E_{00} \gg kT$ for FE, $E_{00} \sim kT$ for T-FE, and $E_{00} \ll kT$ for TE. The major barrier height (E_B) dependence is contained in $R_0(\propto J_s^{-1})$ with $R_0 \propto e^{E_B/E_0}$.

Current-voltage characteristics at 4.2 K for the three 1×10^{18} n-$\mathrm{In}_x\mathrm{Ga}_{1-x}\mathrm{As}$ $(x = 0.07, 0.10, 0.15)/2\times10^{16}$ n-GaAs samples are shown in Fig. 2, illustrating the exponential increase in current level with decreasing barrier height. In curve (a), for the sample with the highest barrier height ($\simeq$125 meV), the foreward I-V relationship is exponential over much of the range of the figure. At higher voltages, which are a substantial fraction of the barrier height, the diode is so conductive that the current is limited by series resistance in the sample, causing a downward curvature in the I-V. In curves (b) and (c), representing lower barrier heights, this occurs at lower voltages, due to the increased conductance of the devices, so that no clear region of exponential dependence is evident. Scaling the current by multiplying by the zero-bias resistance eliminates most of the barrier height dependence, so that the JR_0 vs V characteristics should be almost identical at low voltages. This was observed in these samples, which were identical except for the difference in Schottky barrier height (see Fig. 1).

The current-voltage characteristics of a number of samples were studied at temperatures ranging from 4.2 to $\simeq$200 K (junction conductance was too large at higher temperatures, even with the largest barrier heights studied, and conductances were limited by other parts of the structure). The I-V characteristics were fit using the theory of Padovani and Stratton[12] for the FE and T-FE regimes. Using the value of E_{00} obtained by fitting the exponential part of the characteristics at 4.2 K, barrier heights were extracted which were within $\simeq$10% of the value obtained from the simulations (i.e., from solving Poisson's equation for the heterostructure), at least for samples with barrier heights (E_B) in excess of $\simeq$100 meV. For samples with smaller barrier heights, the I-V's yielded larger values of E_B than the simulations, so that the samples were less conductive than expected. For low barrier heights, there are several possibly important effects, such as the effect of free carriers on the space charge,[12] and the fact that the "metal" in these Schottky barriers is actually a degenerate semiconductor, which were ignored. Also, the depletion width is reduced to lengths approaching the interdonor spacing. For a 50-meV barrier, the depletion width in 2×10^{16} GaAs, even at zero bias, is only $\simeq$2 interdonor spacings. Thus, the theory is expected to break down for very low barrier heights. However, it is clear that our samples had barriers of small and controllable height.

The temperature dependences of the parameters R_0 and J_s were in agreement with theory in the FE and T-FE regimes. The value of E_0 increased more rapidly than expected in the T-FE regime, and appeared to approach $E_{00} \propto nkT$, with $n \simeq 1.6$. An increase in E_0 with temperature beyond that expected for a parabolic barrier is consistent with image force lowering of the barrier.[13] In all samples, the 4.2-K values for E_{00} obtained from the I-V curves were larger than expected for the known sample dopings. With image force lowering included, evaluation of the WKB tunneling probability using the known sample doping gave values of E_{00} close to those actually observed. The behavior of the I-V parameters, including their temperature dependence, confirms that these heterojunction devices behave as Schottky barrier diodes.

In conclusion, we have demonstrated for the first time Schottky barrier diodes with continuously adjustable barrier heights, down to the millivolt (30–150 meV) level. In these n^+-InGaAs/n-GaAs heterojunctions the barrier height is controllable primarily through two fabrication parameters, the doping and composition of the n^+ layer. Conduction at small biases in diodes with barrier heights in excess of $\simeq$100 meV could be accounted for by the theory of tunneling and temperature-assisted tunneling in Schottky diodes. At larger biases, in the exponential region of the I-V characteristic, the magnitude and temperature dependence of the exponent were both larger than expected, probably due to image force lowering of the barrier. For lower barrier heights (below $\simeq$100 meV), the behavior of the diodes was qualitatively similar to those with larger barriers; however, the increase in diode conductance with decreasing barrier height, although exponential, was somewhat slower than expected. Several physical effects, including the breakdown of the uniform doping model of the semiconductor depletion region as the depletion width approaches the average interdonor spacing, have not been taken into account, and illuminate the possibility of interesting physics in this new regime of millivolt barriers. Finally, these devices offer an alternative to metal-semiconductor Schottky barriers, in which the barrier height is determined by Fermi level pinning.

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