Superconducting InGaAs junction field-effect transistors with Nb electrodes

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We describe the design, fabrication, and characterization of superconducting $In_{0.47}Ga_{0.53}As$ junction field-effect transistors (JFETs) with Nb source and drain electrodes. $In_{0.47}Ga_{0.53}As$ has the advantage of combining large coherence length and high Schottky barrier transmission, making it a very attractive material on which to base superconducting FETs. At large voltages these devices behave as normal FETs in either enhancement or depletion modes, while at small voltages they act as Josephson junctions or super-Schottky diodes. Both normal and supercurrents are controlled by the gate.

A field-effect transistor (FET) in which the source and drain metallizations are superconductors can exhibit superconducting properties (at source-drain voltages of order the electrode energy gap) which are controlled by varying the gate voltage. In short-channel devices with suitable superconductor-semiconductor contacts, the channel becomes superconducting by the proximity effect, and Josephson effects occur. Such Josephson FETs (JOFETs) were first proposed over a decade ago.[1] Recently, gate-controlled supercurrents have been demonstrated,[2] and true superconducting FETs, exhibiting a wide range of gate control of both super and normal currents, have been built.[3] In this letter, we report on the design, fabrication, and initial characterization of superconducting $In_{0.47}Ga_{0.53}As$ junction field-effect transistors (JETs) with Nb electrodes. These are the first junction-type JOFETs and the first JOFETs based on this very attractive materials system.

At this early stage of research on JOFETs, the choice of superconducting electrode material is of secondary importance; Nb was used for this work. The major materials-related concern is the choice of semiconductor. The semiconductor materials system chosen should be one which allows the fabrication of high quality FETs. Beyond that most basic concern, this work was motivated by a desire to address two fundamental issues which dominate JOFETs: (1) The channel length scale, which is set by the normal coherence length of the semiconductor, and (2) the superconductor-semiconductor source and drain contacts, in particular the transmission coefficient for tunneling through the Schottky barriers. $In_{0.47}Ga_{0.53}As$, grown epitaxially on InP substrates, was chosen as the semiconductor for this work because it offers large coherence lengths and Schottky barrier transmission coefficients, as discussed in the following paragraphs.

(1) In order to have a supercurrent in a JOFET, the separation L of the source and drain electrodes must be no more than a few times the normal coherence length ξ_n in the semiconductor channel since, under typical conditions, the critical current I_c varies as $\exp(-L/\xi_n)$. For a material with Fermi velocity v_F, carrier diffusion constant D, and elastic mean free path l, ξ_n is given by $\hbar v_F/2\pi k_B T$ and $(\hbar D/2\pi k_B T)^{1/2}$ in the clean ($l \gg \xi_n$) and dirty ($l \ll \xi_n$) limits, respectively. In both cases $\xi_n \propto v_F = \hbar k_F/m^*$, where m^* is the carrier effective mass, and the desire to maximize ξ_n leads to the selection of low effective mass materials. In n-type InAs, $In_{0.47}Ga_{0.53}As$, GaAs, and Si, the values of ξ_n have the ratios 3.4:2.4:2.0:1 in the dirty limit, for a given carrier concentration and mobility. (Of course, the larger mobilities in low mass materials make these ratios even larger.) In the clean limit, the corresponding ratios are 11.3:5.9:3.9:1, again for fixed carrier density. InAs materials technology is not well developed, and high quality FETs are very difficult to obtain, and we therefore chose $In_{0.47}Ga_{0.53}As$ for this work.

(2) The superconductor-semiconductor interfaces should be as transmissive as possible.[4] This led early workers[1] to suggest InAs as a suitable material, since Schottky barrier-free contacts are possible. For materials with which high quality FETs have been built, Schottky (tunneling) barriers at metal-semiconductor contacts are expected. Supercurrent transport in JOFETs is a coherent process involving two tunneling events (one at each superconductor-semiconductor interface) so the critical supercurrent is proportional to P^2, where P is the transmission probability for a single interface. In the WKB approximation,[5] $P = \exp(-E_B/E_{00})$, where E_B is the Schottky barrier height and $E_{00} = (e\hbar/2)(N_D/\epsilon_s m^*)^{1/2}$, with N_D, ϵ_s, and m^* being the dopant density, dielectric constant, and carrier effective mass of the semiconductor, respectively. For n-type $In_{0.47}Ga_{0.53}As$, GaAs, and Si, using barrier heights of 0.2, 0.7, and 0.2 eV, we have $P^2 = 9.2\times10^{-2}$, 3.4×10^{-6}, and 4.6×10^{-5}, respectively, for a carrier density of 5×10^{19} cm^{-3} at the interface. Again, $In_{0.47}Ga_{0.53}As$ appears to be desirable for JOFET devices, compared with other materials from which FETs are fabricated. It is the combination of low barrier height and low carrier mass relative to the other materials which is responsible for this great disparity in favor of $In_{0.47}Ga_{0.53}As$ (the disparity increases with decreasing doping). Although the WKB approximation breaks down for large doping,[6] this calculation should indicate the correct qualitative trend.

Most studies of JOFETs and ungated semiconductor-coupled weak links have focused on the coherence length in the semiconductor through measurements of the critical current. Systematic studies of the influence of the contact properties are only beginning. In contrast to the situation with normal FETs, the superconductor-semiconductor contacts in JOFETs have an importance as great as that of the contacts between the gate and the channel. Thus we chose

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for our initial studies an inverted device structure, with the gate underneath the channel, allowing the superconductor to be deposited on the as-grown semiconductor surface. The device is a JFET with a p-type $In_{0.47}Ga_{0.53}As$ gate. A depletion-mode device is illustrated schematically in Fig. 1. The channel is conducting in absence of gate bias. Application of a negative voltage to the gate terminal (with the source grounded) increases the width of the gate depletion region (shaded in Fig. 1), thereby decreasing the conducting channel thickness, and eventually pinching it off completely. Application of a positive gate voltage increases the channel width. Enhancement-mode devices, which are pinched off at zero gate bias, were also built.

The $In_{0.47}Ga_{0.53}As$ layers were grown on a p^+-InP substrate by molecular beam epitaxy (MBE). At the time of this work, we were unable to deposit the Nb film in the MBE system. The wafers were transferred to a separate system immediately after growth of the $In_{0.47}Ga_{0.53}As$ layers, and Nb was deposited by electron beam evaporation. Device mesas were etched by ion milling. A narrow gap between the Nb electrodes was defined by reactive ion etching using an NF_3-based chemistry and an Al mask, which was patterned by optical lithography and liftoff. The minimum source-drain separation on the photomask was 0.5 μm.

Design values for the layer thicknesses and dopant densities for the initial fabrication run are shown in Fig. 1. The gate depletion layer thickness is estimated to be 64 nm (21 nm on the n side), leaving a channel thickness of 49 nm. Low-temperature Hall measurements were consistent with this, with a Hall mobility of 2500 cm^2/V s. Calculated device parameters include 510 $\Omega/\square$ resistance (0.51 Ω mm for a 1-μm-long channel), 50 nm electron mean free path, and 62 nm coherence length at 4.2 K.

The 5 nm n^+ layer was used to ensure good ohmic contacts. Based on a Schottky barrier height of $\sim$0.2 eV, this layer is completely depleted of carriers over the entire device, as indicated by the shading in Fig. 1. Thus it improves

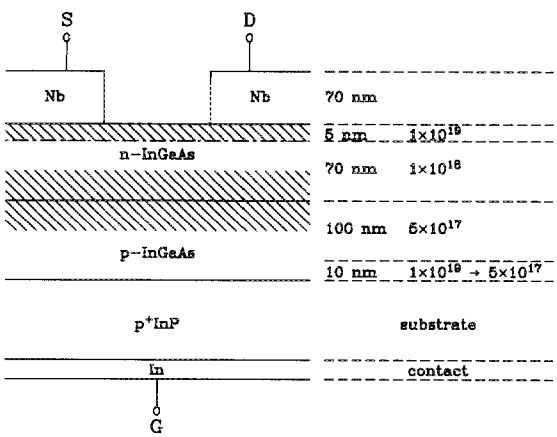

FIG. 1. Schematic of inverted-gate JFET structure. The left portion of the figure illustrates the vertical structure, with the source (S), drain (D), and gate (G) terminals indicated. Regions depleted of carriers are shaded. The clear n-type region in between is the channel. At the right, the layer thicknesses and dopings (in cm^{-3}) for the first fabricated device are shown. Note the use of a thin, heavily doped contact layer, which is completely depleted and does not participate in lateral current transport, but which reduces the thickness of the contact Schottky barriers.

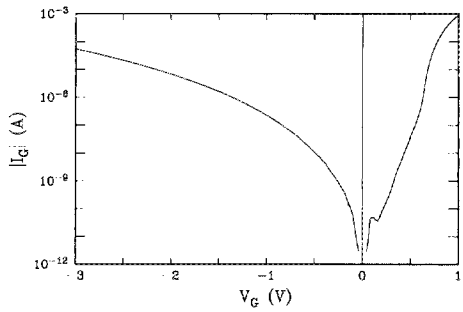

FIG. 2. Magnitude of gate current vs voltage for a typical large-area p-n junction at 4.2 K. Note the negative-resistance feature associated with interband tunneling in the forward direction. The low leakage of these junctions allows several volts of reverse bias to be applied, pinching off the conducting channels of the FETs.

electron transmission at the contact interface without contributing to lateral current transport.

Large-area gates were used in this work in order to simplify the fabrication process. Device mesas were etched into the p-$In_{0.47}Ga_{0.53}As$ layer. Heavy doping was used at the interface between InP and $In_{0.47}Ga_{0.53}As$ in order to minimize its contribution to the gate characteristics. The current-voltage (I-V) characteristics of a representative large-area ($>10^{-4}$ cm^2) gate are shown in Fig. 2. The low leakage of these p-n junctions is important to the function of the JFETs. The gate current is due to interband tunneling. Forward gate bias, which increases the conducting channel thickness, is limited to less than $\sim$1 V, but several volts can be applied in the reverse direction, depending on the doping of the p and n layers. A device designed with a sufficiently thin channel can be completely pinched off.

The source-drain I-V characteristics of a representative depletion-mode JFET, for several values of gate voltage at 4.2 K, are shown in Fig. 3. On the voltage scale shown, the device acts as a normal JFET[7]; the fact that the electrodes are superconducting does not significantly alter the characteristics. In this particular device, the doping was low enough that the channel was pinched off with a reverse gate bias of $-$1 V, and a forward bias of $\simeq$1 V could be applied without excessive gate current.

When cooled below the electrode transition temperature, the characteristics of virtually all of the devices we have studied exhibit effects due to superconductivity in the source and drain electrodes. The effects were limited to a voltage

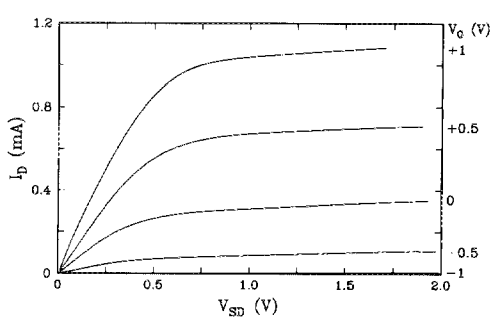

FIG. 3. Source-drain I-V characteristics of a representative JFET at 4.2 K for various values of gate bias. On a scale of volts, these devices behave as ordinary FETs, with channel conductance and saturation current controlled by the gate. In this enhancement-mode JFET, positive (negative) voltages increase (decrease) channel current.

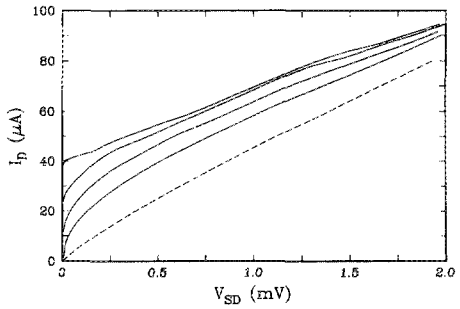

FIG. 4. Source-drain I-V characteristics of a JFET which exhibits a supercurrent at 1.6 K. Note the 1000 times reduction of the voltage scale compared with Fig. 3. On this scale, $I(-V) = -I(V)$. In the device shown, a gate-controlled supercurrent is seen, along with an excess current and a conductance peak at subgap voltages (solid curves, for $V_G = 0$, -2, -2.5, and -3 V). The dashed curve was taken above the electrode transition temperature with no gate bias.

scale which is on the order of the superconducting energy gap of the electrodes. Devices with relatively high resistances act as back-to-back super-Schottky diodes,[8] exhibiting an increased resistance at subgap voltages. Their characteristics are dominated by tunneling between the superconducting electrodes and the normal channel through the Schottky barriers at the contacts. The tunneling current at each contact is suppressed for contact voltage drops smaller than the superconducting energy gap due to the absence of states in the superconductor at subgap energies.

Low-resistance devices (those having very transmissive or low resistance contacts) with short channels exhibit gate-controlled Josephson supercurrents. Figure 4 shows the I-V characteristics for one such device on a mV scale (a 1000-fold sensitivity increase in the voltage scale compared with Fig. 3). The four solid curves in the figure are for gate voltages of 0, -2, -2.5, and -3 V at 1.6 K. Gate current was negligible. In this particular device, the relatively high channel doping, close to that indicated in Fig. 1, led to a large supercurrent. However, the channel could not be pinched off completely. Greater sensitivity to gate voltage was achieved in devices with somewhat lower channel dopings and shorter channels (in the present work such channel lengths were at the limit of what we could attain with optical lithography). Thus, both gate-controlled supercurrent and channel pinchoff have been observed in the same device. The dotted curve in Fig. 4 was obtained at 10 K (above the electrode transition temperature T_c) with no applied gate voltage. Below T_c, the current was linear in voltage for voltages much larger than the superconducting energy gap, exhibiting an excess current when extrapolated back to zero voltage. This behavior is common in superconducting junctions involving normal metals, and is due to Andreev scattering at the superconductor-normal metal interface(s).[9]

Typical critical current-normal resistance products $I_c R_n$ in these devices varied between 1 and 2 mV at low temperatures. This is close to the value expected for an ideal Josephson junction with Nb electrodes (2.4 mV). In semiconductor or normal metal-coupled junctions, this value should be reduced by a factor of order $\exp(-L/\xi_n)$, where L is the electrode separation and ξ_n is the normal coherence length.[4,10] In these devices, L was 0.5–1 μm (recall that optical lithography was used to define the electrodes), and ξ_n was estimated to be 90 nm at 2 K, so that the expected $I_c R_n$ product is less than ~ 10 μV. This sort of discrepancy has been reported by a number of workers in semiconductor-coupled weak links reported by a variety of workers, and is an important subject for future investigations. Resistances in the devices exhibiting supercurrents were consistent with expectations for channels of the measured dimensions and carrier densities. Thus it is the critical current which is anomalously large in these devices. Critical currents in devices of this type are known to be very sensitive to contact quality. Thus, we have been able to obtain the very high quality contacts expected with this materials system.

In conclusion, we have fabricated superconducting JFETs with Nb electrodes, based on $In_{0.47}Ga_{0.53}As$ lattice matched to InP substrates. $In_{0.47}Ga_{0.53}As$ appears to represent a well-optimized choice of a semiconductor material on which to perform device investigations, due to the highly transmissive contacts and long coherence lengths which are possible. The devices reported on here represent a good starting point for the study of JOFETs in this materials system. Understanding of the behavior of Josephson FETs and semiconductor-coupled weak links has been hampered by a lack of experiments on well-defined structures (e.g., with known length, channel thickness, carrier concentration, and mobility), which can be compared with theory in detail. The structure described here is one which makes such investigations possible. Finally, the largest problem with JOFETs, when considering possible applications, is the large disparity between the input (gate) and output (source-drain) voltage scales.[11] In the future, we hope to reduce the gate voltage swing required to pinch off the devices by optimizing doping and channel thickness.

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