Reduced reverse bias current in Al–GaAs and $In_{0.75}Ga_{0.25}As$–GaAs junctions containing an interfacial arsenic layer

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(Received 10 February 1987; accepted 21 April 1987)

Interfacial As is shown to reduce reverse-bias current in Al–GaAs Schottky barriers. It is suggested that the leakage reduction is associated with the removal of low work function phases at the interface. In addition, current–voltage measurements performed on $In_{0.75}Ga_{0.25}As$–GaAs heterojunctions indicate a dependence upon the condition of the GaAs prior to deposition of the $In_{0.75}Ga_{0.25}As$ layer.

I. INTRODUCTION

Excess reverse bias current in metal–semiconductor contacts can degrade device performance. For example, gate current limits field-effect transistor (FET) sensitivity and increases power consumption. In charge-coupled device applications, gate current can contribute to dark current and introduce nonlinearity in charge packets, thus reducing the signal-to-noise ratio. Reverse bias current reduction in GaAs devices requires insight into the relationship among chemical, structural, and electrical properties of the metal–semiconductor interface. A manifestation of the interaction among these properties is the phenomenon of Fermi-level pinning.

Understanding Fermi-level pinning, however, remains a formidable problem. Models which attempt to describe this behavior include metal-induced gap states (MIGS),[1] extrinsic defect generation during adatom deposition,[2] and effective work functions of mixed interface phases resulting from chemical reactions between metal and semiconductor.[3] The effective work function (EWF) model asserts that these reactions primarily result in excess anion precipitates (e.g., arsenic) which dominate the interface behavior and thus dictate the effective work function. If low work function regions exist at the unannealed interface they could reduce the effective work function and observed barrier height, noticeably increasing the reverse bias current. Ohmic behavior, for example, has been reported from a low-work function phase of Au–Ga that forms at the periphery of an annealed Au–GaAs contact.[4] Reduction or elimination of these low-work function areas should reduce the reverse bias current. This paper reports an attempt to reduce reverse bias current in Al–GaAs Schottky diodes by creating a homogeneous interface through deposition of an arsenic layer prior to metallization. In addition, the electrical properties of an $In_{0.75}Ga_{0.25}As$–GaAs junction have been examined and are shown to be dependent upon the condition of the GaAs surface prior to deposition of the InGaAs layer.

II. Al–GaAs JUNCTION

In this experiment, a molecular beam epitaxy (MBE) system is used to grow an Al–As–GaAs "test" structure and an Al–GaAs "control" structure. After initial preparation, an n^+ GaAs sample was mounted onto a Mo block using In and loaded into the MBE chamber. Subsequent heating removes the native oxide and helps form a backside ohmic contact. A 0.5-μm, 2×10^{18} cm^{-3} n-GaAs buffer layer is grown followed by an additional 0.5-μm n-GaAs layer doped at 2×10^{17} cm^{-3}. The "test" structure was allowed to cool to room temperature and then exposed to an As_2 flux for a time corresponding to the deposition of 100 Å of As, assuming a unity sticking coefficient. Prior to removal from the chamber, 1800 Å of Al was evaporated on both samples. Diodes were defined by photolithography and wet chemical etching. The maximum temperature during these latter procedures was 90 °C which should avoid any annealing effects that could degrade the As interlayer's homogeneity.

Current–voltage (I–V) characteristics were measured at room temperature, and the barrier height and ideality calculated from the forward bias data using a least-squares fit. A typical comparison between the "test" and "control" structures is depicted in Fig. 1, indicating that the sample contain-

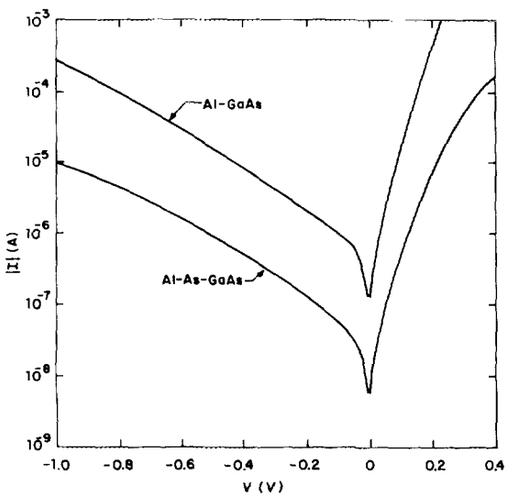

FIG. 1. Comparison between Al–GaAs and Al–As–GaAs I–V characteristics showing large reduction in reverse leakage current.

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TABLE I. Ideality factor, barrier height, and leakage current density at 1 V reverse bias for representative samples.

Sample	Barrier height (eV)	Ideality	Current density at −1 V (mA/cm^2)
Al/GaAs	0.65	1.06	31.12
Al/As/GaAs	0.70	1.20	1.10
1(a)	0.65	1.47	0.86
1(b)	0.60	1.03	3.53
2(a)	0.66	1.01	0.11
2(b)	0.51	1.07	70.70

ing the As interlayer exhibits a 25-fold reduction of reverse-bias current. Table I compares the barrier height, ideality, and current density for the two samples. The test structure, while displaying less ideal behavior, does in fact have a typically 50–60 mV greater barrier height to accompany the reduced current. The difference in barrier heights has been confirmed by internal photoemission measurements. Although roughly an 80 mV barrier height enhancement would be necessary to account for the current reduction, the measured barrier height difference is within the experimental error. Reverse bias current reduction, therefore, has been achieved by generating a more uniformly pinned interface.

Indeed, the coincidence of As and reduced-dark current has been previously observed[5]. Ostensibly contradictory data for Al on arsenic-rich GaAs surfaces also exists.[6] Wang showed that increasing As-surface coverage is associated with a concomitant decrease in the Al-barrier height to GaAs. It was also shown, however, that the opposite is true for Al on AlAs possibly due to the fact that intermixing of Al and Ga is precluded in the AlAs case. It is likely that Al and Ga intermixing does not occur for the thick-As layer used in this experiment and thus, the apparent contradiction can be explained.

It might also be possible to associate the reduced current with a metal–insulator semiconductor (MIS) model of the junction. This effect is improbable since the current reduction is a constant factor nearly independent of the applied voltage. Experiments to differentiate between various models of the reverse current transport mechanism are in progress.

III. $In_{0.75}Ga_{0.25}As$–GaAs HETEROJUNCTION

The influence of the GaAs-surface condition on the measured InGaAs–GaAs barrier height was also investigated. MBE was used to grow a 0.5-μm-GaAs buffer layer on a semi-insulating substrate followed by a 0.5-μm, 5×10^{16} cm^{-3} n-GaAs layer. At this point, four different sample preparations followed:

1(a) Approximately 100 Å of As was deposited at room temperature between the GaAs and the intrinsic InGaAs, the latter of which was grown at 200 °C.

1(b) Intrinsic InGaAs was grown on the GaAs at 450 °C.

2(a) The sample was removed from the chamber and air exposed. It was then reinserted and intrinsic InGaAs grown at 200 °C.

2(b) This sample was also air exposed. The InGaAs-growth temperature, however, was 350 °C which should desorb the As oxide at the GaAs surface.[7]

In all samples, the intrinsic InGaAs layer is 0.2-μm. The samples are schematically represented in Fig. 2. After the InGaAs growth, 180-μm-diam Au contacts were evaporated onto the InGaAs through a stainless steel mask in a deposition system having a base pressure of 1×10^{-7} Torr. Probing between Au contacts before mesa etching the InGaAs layer yields ohmic behavior indicative of a low barrier contact of the Au to the intrinsic InGaAs. After mesa etching, the I–V characteristic resembles that of two back-to-back diodes. Ohmic contacts were formed by alloying In to the GaAs at 300 °C in forming gas using a rapid thermal annealer. Before measuring the rectifying behavior of the

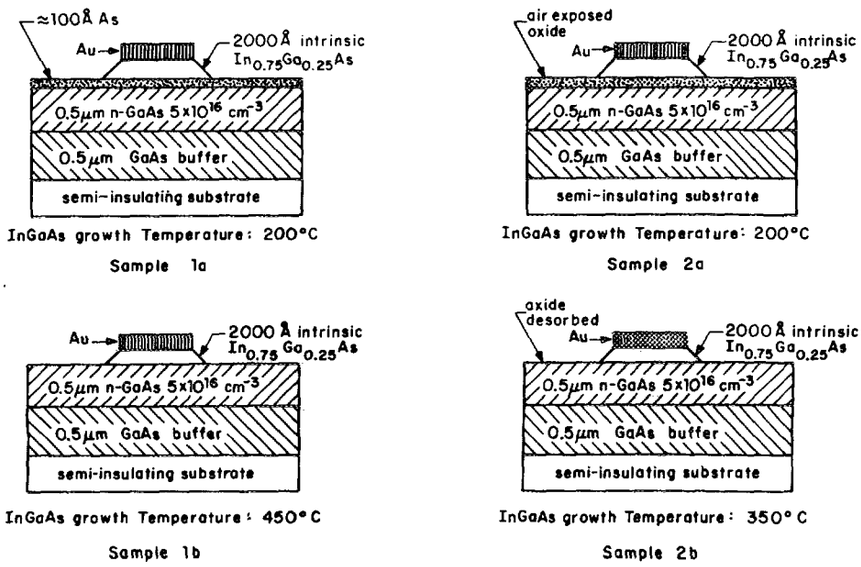

FIG. 2. Schematic cross section of the $In_{0.75}Ga_{0.25}As$–GaAs junctions. Samples 1(a) and 1(b) were grown entirely under UHV conditions. Samples 2(a) and 2(b) were air-exposed prior to InGaAs deposition. Au was evaporated after removal from the MBE chamber.

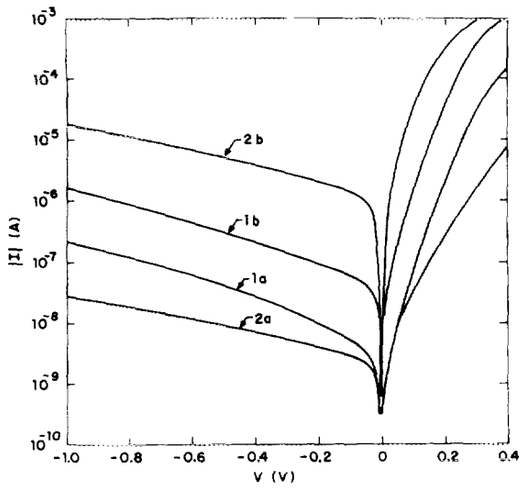

FIG. 3. *I–V* characteristics for $In_{0.75}Ga_{0.25}As$–GaAs junctions indicating a strong dependence on the GaAs surface condition.

InGaAs–GaAs junction, the characteristic between two Au contacts as well as the integrity of the In contacts were confirmed.

Typical *I–V* characteristics for the four samples are shown in Fig. 3, while the barrier heights and ideality factors are summarized in Table I. The samples possessing interfacial As, whether elemental or in oxide form, exhibit current reduction. Specifically, the InGaAs–As–GaAs sample has four times less current at 1-V-reverse bias than the InGaAs–GaAs case. More dramatically, for the air-exposed samples the one in which the As oxide was desorbed has roughly a factor of 640 greater current than the sample grown at lower temperature. In fact, the air-exposed low temperature growth sample has the lowest reverse bias current of all samples tested as well as the best ideality factor. Furthermore, the barrier heights for the InGaAs–As–GaAs sample and the air-exposed sample possessing the As oxide are nearly equivalent to within the 10-mV deviation in measurement. The lowest barrier height is associated with the air-exposed sample in which the As oxide was desorbed.

IV. SUMMARY

Leakage current in Al–GaAs Schottky diodes has been reduced by the introduction of an interfacial As layer. While this effect does not preclude other models of the metal–semiconductor interface, it does support the premises of the effective work function model in which the barrier height reflects an average work function of mixed phases and As is believed to pin the interface Fermi level. The measured barrier height of the $In_{0.75}Ga_{0.25}As$–GaAs heterojunction has also been shown to depend upon interfacial As, regardless of the As phase. Investigation of leakage current reduction not only lends insight into the interface but may also have practical implications for threshold voltage control and sidegating in GaAs integrated circuits.

ACKNOWLEDGMENTS

The authors thank Dr. Norman Braslau of IBM Research for the internal photoemission measurements. This work is supported by an IBM Faculty Development Award (ERF) and an IBM Graduate Fellowship (DVR) as well as by the Joint Services Electronics Program under Contract No. DAAG29-85-K-0049.

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