III-V Compounds and Alloys: An Update
Author(s): Jerry M. Woodall
Reviewed work(s):
Source: *Science*, New Series, Vol. 208, No. 4446, Advanced Technology (May 23, 1980), pp. 908-915
Published by: American Association for the Advancement of Science
Stable URL: http://www.jstor.org/stable/1683600
Accessed: 25/02/2013 12:12

Your use of the JSTOR archive indicates your acceptance of the Terms & Conditions of Use, available at http://www.jstor.org/page/info/about/policies/terms.jsp

JSTOR is a not-for-profit service that helps scholars, researchers, and students discover, use, and build upon a wide range of content in a trusted digital archive. We use information technology and tools to increase productivity and facilitate new forms of scholarship. For more information about JSTOR, please contact support@jstor.org.

American Association for the Advancement of Science is collaborating with JSTOR to digitize, preserve and extend access to *Science*.

http://www.jstor.org

This content downloaded on Mon, 25 Feb 2013 12:12:51 PM
All use subject to JSTOR Terms and Conditions

III-V Compounds and Alloys: An Update

Jerry M. Woodall

Nowadays, meaningful discussions of solid-state materials are usually coupled to their function, either for the study of solid-state phenomena or for use in the realization of a device. This is particularly true for semiconductor materials. Nearly all research on the preparation of semiconductor materials is motivated by anticipated advantages from their use in advanced device technology, and it is rare to find such research in this field for its own sake. A semiconductor research several that have been demonstrated using III-V's, for only a few—microwave devices and light-emitting diodes (LED's)—have economic processing procedures been developed.

To focus in more detail on this issue, I compare in Table 1 some relevant properties of silicon with those of the III-V compound GaAs, a material widely researched and currently used in commercial devices. At first glance, those who recognize the significance of these

Summary. The III-V compounds and alloys have been studied for three decades. Until recently, these materials have been commercialized for only a few specialized optoelectronic devices and microwave devices. Advances in thin-film epitaxy techniques, such as liquid phase epitaxy and chemical vapor deposition, are now providing the ability to form good quality lattice-matched heterojunctions with III-V materials. New optoelectronic devices, such as room-temperature continuous-wave injection lasers, have already resulted. This newfound ability may also affect the field of high-speed integrated circuits.

effort usually considers the material, the device, and processing as a unit. It is within this framework that III-V (*1*) compound semiconductor research has evolved.

From a commercial point of view, the current economic impact of III-V materials is barely noticeable. As is well known, the semiconductor world is dominated by silicon devices. This is because silicon devices and integrated circuits are the result of an optimal combination of material properties and reliable low-cost processing methods. Optimal combination is the key consideration (*2*), for no matter how exciting the transport or optical properties of some newly made material are, it will never see the marketplace unless an economically competitive device, circuit, or electronic system can be made from it. The III-V materials have not yet effectively competed with silicon, for of the many devices that have been conceived and the

The author is a research staff member at IBM T. J. Watson Research Center, Yorktown Heights, New York 10598.

properties in terms of potential device performance might wonder why silicon is used at all (*3*). For instance, the direct band gap implies high radiative recombination efficiencies (efficient light-emitting devices). The larger band-gap energy generally means higher device operating temperatures. Higher carrier mobilities and larger electron saturation drift velocities suggest transistors with higher speed or lower power dissipation. However, there are factors not shown in Table 1 that are equally important. First, silicon is a very abundant element and is easily refined into a high-purity form. Silicon can be easily converted into bulk single crystals of almost any desired size and shape and then sliced into wafers with dimensions that facilitate economic device processing. The thermally grown oxide of silicon, SiO_2, used for passivation and several device structures is both electronically and chemically superior to the oxides grown on GaAs. The control of the electronic properties of silicon during processing is superior to that of GaAs. Simply stated, silicon has a better rust than GaAs and can be more reliably processed into intricate devices.

Nevertheless, in the research and development laboratory, III-V materials work is very visible and appears to be increasing. In view of the commercial position of silicon, it may well be asked (particularly by board members of companies researching III-V materials) why. Several compelling reasons justify this research. First, some of the III-V materials have electrical properties that should lead to transistor devices with significantly higher performance than those made with silicon. Second, most III-V materials have optoelectronic properties that silicon does not have, and hence can be made into devices with unique or exclusive functions—for example, injection electroluminescence and injection lasing. Third, the III-V compounds can be alloyed or mixed together. This allows the formation of material with continuously variable properties, such as band-gap energy, charge carrier mobility, and lattice constant, and adds several new dimensions in the design and function of new device structures. For example, lattice-matched heterojunctions formed between III-V compounds or alloys with different band gaps can confer optical, electrical, and chemical advantages over silicon devices and circuits. When these advantages are considered for transistor devices and circuits, it is quite likely that this will lead to improved processing methods with better reliability, lower cost, and higher yields. The implications of this possibility have been partly responsible for a resurgence of research on III-V materials applied to data-processing devices and circuits. This article highlights some of the advances in III-V materials and devices that have led to this situation. As this discussion cannot be comprehensive, the material presented will reflect to some degree the biases of the author.

Structures and Devices

To put into proper context the discussion of the advances in materials preparation techniques, it is useful to describe some generic structures and phenomena related to a broad class of devices, particularly optoelectronic devices based on heterojunction structures.

It is not overstating the case to say that over the past 15 years the major impact of III-V materials has been in the area of optoelectronic devices and that one of the most important reasons for this has been the development of the

0036-8075/80/0523-0908$02.00/0 Copyright © 1980 AAAS

This content downloaded on Mon, 25 Feb 2013 12:12:51 PM
All use subject to JSTOR Terms and Conditions

ability to epitaxially form good quality latticed-matched heterojunctions between dissimilar materials in a controllable and reproducible fashion. In my opinion, this accomplishment represents the single most important advance to date in the field of III-V materials science and technology.

Most of the beneficial aspects of lattice-matched heterojunctions can be generically understood by considering Fig. 1. A somewhat schematic representation of an energy band diagram for a typical III-V material is shown in Fig. 1a. The ordinate direction represents electron energy and the abscissa direction represents a spatial coordinate. The lines marked E_c and E_v show the energies of electrons in the bottom of the conduction band and the top of the valence band, respectively, as a function of position in the crystal. The termination points of these lines are the crystal surfaces. The line marked E_f is the Fermi energy level and is uniform throughout, indicating no net current flow. In this example, E_f is near the bottom of the conduction band in the interior of the crystal, indicating that the crystal is *n*-type and hence electrons are the majority carrier. Notice that the lines E_c and E_v are parallel throughout and are bent upward at the surface of the crystal. This is due to a large density of surface states associated with the native oxides present on III-V material surfaces. These states are distributed between E_c and E_v and can trap both electrons and holes near the surface. If the crystal is *n*-type, the states will trap electrons, producing a negative charge on the surface. This negative charge is balanced by the positive charges, due to the ionized donors stripped of their electrons, distributed near the surface. The density of surface states is so large that E_f tends to be "pinned" over a relatively small energy range. This pinning phenomenon is not well understood and is a topic of great interest in the field of surface science. The consequence of the "band bending" due to E_f pinning will become apparent.

Let us introduce a hole—a positive mobile charge—into the crystal near the surface. In a real device, this is accomplished by a hole-injecting junction (a *p-n* junction) or by absorption of a photon. In *n*-type material, holes are minority carriers that greatly perturb the equilibrium state of the crystal, and hence the crystal is eager to eliminate them. One method is direct recombination with electrons, which results in the emission of photons. This occurs, for example, in GaAs and is the mechanism responsible for photoluminescence and injection electroluminescence. Another way to eliminate holes is to have them cross a nearby *p-n* junction, producing a photocurrent. This process occurs in photodetector and solar cell devices. For the situation shown in Fig. 1a, it is most likely that holes near the surface will recombine through the surface states. This represents a loss in most optoelectronic devices and was a very important problem before the development of lattice-matched heterojunctions.

Table 1. Properties of silicon and GaAs relevant to high-speed and optoelectronic device performance.

Property	Si	GaAs
Band-gap energy (eV)	1.1	1.4
Band-gap type	Indirect	Direct
Intrinsic electron mobility (cm²/V-sec)	1,450	10,000
Electron mobility for 10^{17} cm^{-3} (cm²/V-sec)	700	4,500
Electron saturation drift velocity (cm/sec)	1×10^7	2×10^7
Practical *p*-type conductivity for *n-p-n* transistors (ohm-cm)$^{-1}$	16	65

Next consider the lattice-matched heterojunction shown in Fig. 1b. This is similar to Fig. 1a, except that the surface of the *n*-type material, A, has a thin epitaxial *n*-type layer of a lattice-matched material, B, having a larger band gap. In this case, material B was chosen to have the same E_c as material A. As before, let us introduce some holes into material A. In this case, the hole will not be lost by surface recombination. The surface of material A in Fig. 1a is replaced by an interface in Fig. 1b. When a hole approaches the interface, it meets an energy barrier. This barrier is a consequence of material B having a larger band gap than material A. Elimination of the holes will now most likely occur by radiative recombination, unless, of course, the material contains other impurities or defects that act as traps. If we now replace one of the layers of material B with a *p-n* junction, we have one of the basic configurations of currently important optoelectronic devices. If light is absorbed by material A, it acts as an efficient photodetector or solar cell. If the *p-n* junction is electrically forward-biased, it can operate as either an LED or an injection laser.

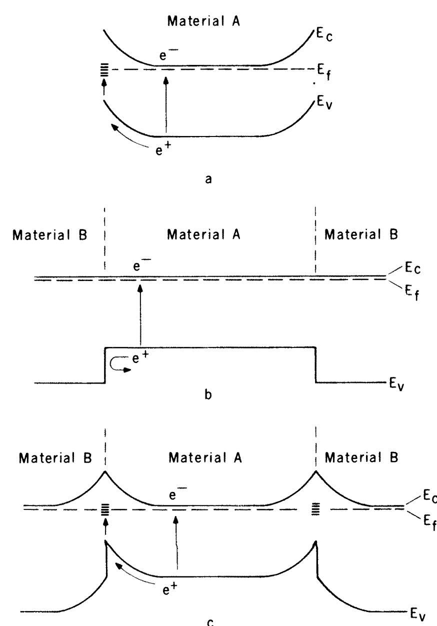

Fig. 1. Energy band diagram of a typical III-V material for three different cases: (a) surfaces with native oxides, (b) surfaces covered with a lattice-matched epitaxial material with a larger band gap, and (c) surfaces covered with a lattice-mismatched material with a larger band gap.

Finally, if the lattice mismatch between material A and material B is sufficiently large (> 0.5 percent), the diagram in Fig. 1c will result. In this example, the surface recombination of Fig. 1a is replaced by interface recombination due to midgap states associated with a density of "misfit" dislocations, which have formed to accommodate the lattice mismatch.

Let us now examine the "menu" of III-V materials available to form heterojunctions. The rich variety of available combinations of band gaps, materials, and lattice constants are shown in Fig. 2. This variety has encouraged the study of ternary and quaternary III-V materials, and the development of epitaxy techniques for these materials has been responsible for many recent advances in optoelectronic devices. The chemical rule that determines the allowable compositions is that the sum of the atom fractions of the group III elements must equal the sum of the atom fractions of the group V elements in the crystal. For example, the ternary alloy of Ga, Al, and As can be expressed as $Ga_{1-x}Al_xAs$, where $0 \leq x \leq 1$, and x is arbitrarily assigned to either of the group III elements. Similarly, the quaternary alloy of Ga, In, As, and P can be expressed as $Ga_{1-x}In_xAs_{1-y}P_y$. The points in Fig. 2 designate "pure" III-V compounds; the lines are ternary alloys that connect two different III-V compounds, whose compositions are expressed as band gaps and lattice constants.

A menu of some widely researched de-

This content downloaded on Mon, 25 Feb 2013 12:12:51 PM
All use subject to JSTOR Terms and Conditions

vice structures is shown in Fig. 3. This figure is a highly schematic representation of generic cross sections of some currently important devices that utilize III-V compounds and alloys. Several of these structures will be discussed in more detail below (*4*). In Fig. 3, E_1 and E_2 refer to materials having different energy gaps, and, except for Fig. 3g, E_1 and E_2 have nearly the same lattice constants. For example, E_1 and E_2 could be either $Ga_{1-x}Al_xAs$ having different x values, or $Ga_{1-x}In_xAs_{1-y}P_y$ having different x or y values, or both (see Fig. 2). Figure 3g refers to a special type of LED made of either $GaAs_{1-x}P_x$ or GaP in which the lattice constant of the substrate, E_1, does not closely match the LED *p-n* junction material, E_2. A layer "graded" in composition from E_1 to E_2 is necessary to prevent the formation of defects that degrade the performance of the LED. It can be seen that except for $GaAs_{1-x}P_x$ and GaP LED's (both of which have significantly affected the small-character-density display business) and GaAs metal-semiconductor field-effect transistors (MESFET's), most of the other devices employ heterojunctions. Of these, an injection laser having two heterojunctions and referred to as the double-heterostructure (DH) laser is perhaps the most unique. Its principles of operation can be understood with reference to Fig. 1b. If one of the material B layers in Fig. 1b is made *p*-type and the other made *n*-type, and the material A layer is made *n*- or *p*-type and about 0.2 micrometer thick, this would describe the most common form of the DH laser. Minority carriers are injected into material A across the *p-n* heterojunction from material B. The other heterojunction "confines" the minority carrier to material A. When the density of the minority carriers exceeds a threshold value, stimulated emission or lasing occurs. The emission is guided out of material A because material B has a lower index of refraction than material A. As a result of the carrier confinement and waveguide properties of the structure, the laser can be made to operate in the continuous-wave mode at room temperature and be modulated at frequencies above 10^9 hertz. This accounts for the development of the use of this type of laser in large-bandwidth optical fiber communication links.

Currently, the most widely studied lasers are those having either GaAs-$Ga_{1-x}Al_xAs$ or InP-$Ga_{1-x}In_xAs_{1-y}P_y$ heterojunction structures. On the other hand, Fig. 2 indicates that it should be possible to use a variety of materials to make devices that lase at wavelengths covering a large portion of the visible and infrared (IR) spectrum. In fact, the wavelengths of interest are those that have the best transmission characteristics in the currently available optical fiber materials. Most of the current research activity is concerned with developing lasers that operate at the desired wavelengths.

Two other optoelectronic devices should be briefly noted: photodetectors and solar cells. As discussed above, these devices produce current or voltage as the result of minority carriers generated by the absorption of light crossing a *p-n* junction. Research on photodetectors is very active, and most of it is directed toward IR devices for military applications. In this field III-V materials do not always have significant advantages over other semiconductors such as II-VI materials. For solar cells the situation is somewhat different. Theoretically, materials with a direct band gap of 1.4 to 1.6 electron volts are the most interesting, and III-V materials of this type have produced solar-to-electrical conversion efficiencies that are equal to and even better than those for silicon. Three of the most notable device structures include *p-p-n* $Ga_{1-x}Al_xAs$-GaAs-GaAs, *n-p* GaAs, and *p-n* InP-CdS cells.

Special mention must be made of GaP and $GaAs_{1-x}P_x$ LED's. Since the early 1970's the visible-wavelength LED has become one of the more technologically important additions to the field of optoelectronic devices. Because of its inherently large energy gap, the first LED's were realized in the GaAs-GaP ($GaAs_{1-x}P_x$) alloy system (see Fig. 2). The most familiar devices have been those formed from $GaAs_{0.6}P_{0.4}$, where the energy gap is direct and strong room-temperature electroluminescence is easily obtained through homojunction formation. These have been used in many alphanumeric display applications and have attained external quantum efficiencies of about 0.1 percent; they emit radiation in the red portion of the spectrum.

Larger gap compositions of $GaAs_{1-x}P_x$ have also been used for LED's. However, because the band gap is indirect for $x > 0.45$ and therefore inherently inefficient for intrinsic radiative recombination, selected "deep-level" impurities must be used for these compositions to assist the recombination process. Historically, GaP was the first indirect material for which selected impurities were used in the fabrication of LED's. The use of zinc and oxygen produced efficient red-emitting diodes, whereas the use of nitrogen (N), a so-called isoelectronic trap, produced efficient green-emitting diodes. These impurities act to confine carriers in their neighborhood. For indirect materials this relaxes the usual crystal momentum selection rules forbidding direct electron-hole recombination and makes the material appear quasi-direct.

These results were then extended to the $GaAs_{1-x}P_x$ system, allowing the fabrication of LED's with a continuously variable emission wavelength. There are commercially available $GaAs_{1-x}P_x$:N LED's that emit yellow and red light. The discovery and utilization of radiation-enhancing impurities in indirect

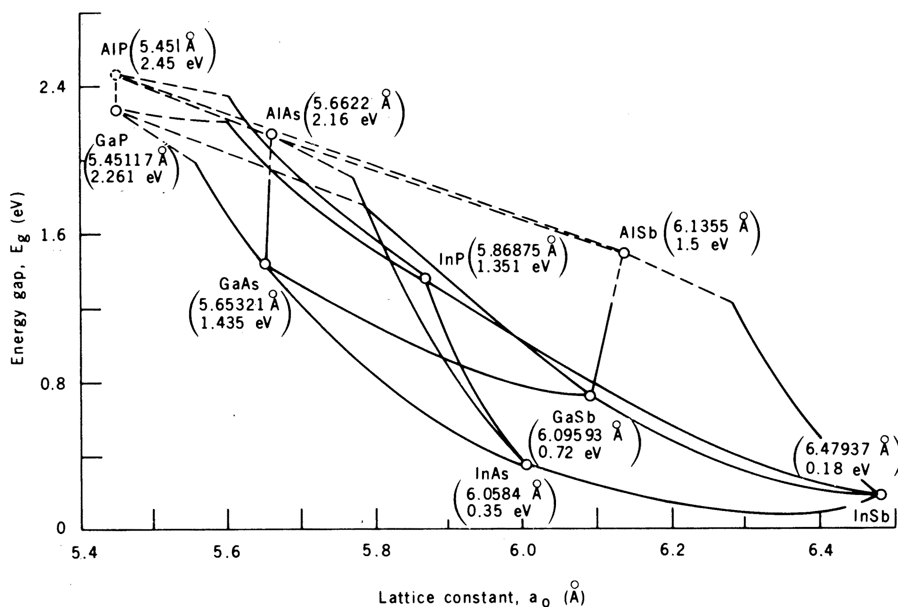

Fig. 2. Diagram representing energy gaps and lattice constants of III-V compounds and ternary alloys.

This content downloaded on Mon, 25 Feb 2013 12:12:51 PM
All use subject to JSTOR Terms and Conditions

band-gap materials has been an important milestone in the development of optoelectronic devices.

So far, this discussion of structure and devices has focused on optoelectronic applications. In the past 3 or 4 years, however, there has been a large increase in research on III-V materials applied to high-speed devices such as field-effect and bipolar transistors. Recently, many integrated circuit functions previously limited to silicon-based structures have been realized in GaAs-based structures. In addition, the performance of most, if not all, of the GaAs circuits—as measured by the product of the dissipated power and circuit delay time, a figure of merit for logic circuits—greatly exceeds that of equivalent silicon circuits. Currently, the most widely researched material and device in this field is the GaAs MESFET, which has a relatively simple structure compared to an injection laser. The basic device consists of a thin *n*-type layer epitaxially grown on or ion-implanted into a semi-insulating substrate. There are two ohmic contacts, the "source" and the "drain," separated by a metal Schottky barrier "gate." An in-depth discussion of the various MESFET structures and their many circuit functions is beyond the scope of this article. It is sufficient to note that varying the voltage on the gate electrode produces a varying resistance to current flow between the source and drain electrodes. Consequently, the materials parameters of primary interest are electron mobility, saturation drift velocity, band gap, and Schottky barrier height. Some of the most important device processing considerations are (i) the reliable production of large, high-purity, semi-insulating GaAs crystals with thermal stability during processing; (ii) a controllable ion implantation technology including thermal activation of dopants; and (iii) Schottky barrier height control.

This discussion of structures and devices has been exemplary rather than comprehensive in nature. It is intended to help put the advances in materials technology described below into proper perspective.

Chemistry and Bulk Crystal Growth

Currently, most semiconductor devices are fabricated on single-crystal substrates of the same material. As a result, there is a demand for reliable bulk crystal growth methods that produce high-quality single-crystal boules of sizes and shapes such that they are easily formed into wafers useful for device processing. For silicon, bulk crystal growth is not considered a problem area. The same is not true for the widely used bulk crystals of III-V materials. The crystal growth problems of these materials can be understood by considering Table 2, which lists some properties of III-V compounds relevant to bulk crystal growth. It can be seen that the advantages of a wide range of band gaps and lattice constants are somewhat offset by the problems presented by the large variations in melting point, dissociation pressure, and chemical reactivity among the compounds. This means that a universal technique or apparatus is not likely to produce the best material for all the III-V compounds. Rather specialized procedures, apparatus, and containment materials must be used for each compound.

To illustrate this point, consider what would happen if the Czochralski method and apparatus for the growth of bulk silicon crystals were used unmodified to grow GaAs. First, how do we get GaAs? For the purpose of bulk crystal growth, the III-V compounds are usually synthesized from the elements. Rapid and efficient synthesis of GaAs occurs when As is added to a Ga melt held at a temperature slightly above the freezing point of the stoichiometric GaAs liquid, ≈ 1240°C. The stoichiometric liquid has an As vapor pressure of about 1 atmosphere in equilibrium with it. Freezing this melt would produce single-phase solid GaAs. Freezing melts with higher or lower As vapor pressures would result in nonstoichiometric GaAs and, in some cases, two-phase material. The second phase could be either occluded Ga or voids due to trapped As vapor or occluded As. Thus an attempt to use the unmodified silicon apparatus for GaAs would result in As evaporating away from the melt and condensing on the colder parts of the apparatus, leaving behind nearly pure Ga. Even if As evaporation were prevented, the melt would become contaminated with silicon because of reaction of Ga with the fused SiO_2 crucible normally used to contain silicon melts. This silicon contamination leads to uncontrolled *n*-type doping in GaAs

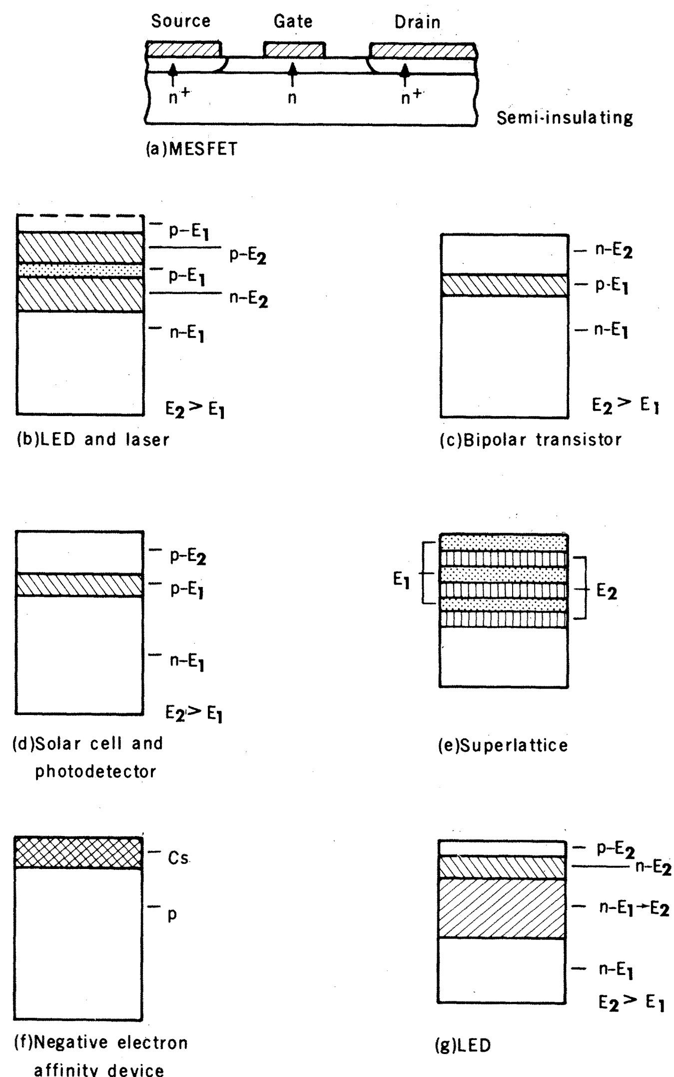

Fig. 3. "Menu" of generic structures for notable devices using III-V materials.

This content downloaded on Mon, 25 Feb 2013 12:12:51 PM
All use subject to JSTOR Terms and Conditions

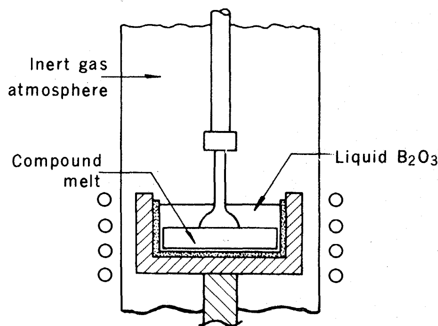

Fig. 4. Schematic of the liquid encapsulation method for bulk crystal growth illustrating the containment of the volatile group V element in the melt.

crystal and is still a topic of research. Thus the thermochemistry of III-V materials plays an important role in the development of bulk crystal growth methods.

In the past, the dissociation problem has been handled with moderate success in the laboratory. The basic solution was to provide a condensing surface for the volatile element (As from GaAs) whose temperature would produce a solid-gas equilibrium vapor pressure equal to that over the stoichiometric liquid—615°C for As solid → $1/4As_4$ gas (1 atm). The remaining internal surfaces of the apparatus were maintained above the condensing temperature. This was accomplished in two widely used devices. One was the modified Czochralski apparatus, which contained internally glass-sealed magnetic lifting and rotating devices. The other was a modified horizontal Bridgman apparatus, which was a sealed fused SiO_2 device with an As "cold" finger at 615°C and a boat, usually made of fused SiO_2, containing the melt at 1240°C.

These two methods adequately served the research community in the past. As the need for device circuit-type substrates has increased, however, so has the need for better crystal growth methods. Several developments have helped to solve this problem, one of which is illustrated in Fig. 4. The technique, called the liquid encapsulation (LEC) method, is essentially the Czochralski method with two important modifications. First, the melt is completely encapsulated by a viscous glass, B_2O_3, which prevents melt dissociation when the dissociation vapor pressure is matched or exceeded by the pressure of an inert gas applied in the apparatus. Second, the apparatus has features common to pressure vessels that contain lifting and rotating feed-through. This apparatus is now routinely used to grow GaAs, InP, and GaP single crystals in sizes useful for device fabrication. The problems that remain for this method applied to GaAs include uncontrolled background impurity contamination and problems with crystal perfection and functional reproducibility. Another technique recently modified to improve size and shape control is the vertical Bridgman or Stockbarger method, shown in Fig. 5. In this method the melt, which is GaP in this example, fills the vessel made of pyrolytically formed BN (Boralloy); B_2O_3 is also used, as it is for the LEC method. The advantage of this method is that the crystal assumes the cross section of the vessel, which can be made circular. Hence the crystal can be sliced into circular wafers, which is very desirable for device processing. This method has been used to grow single crystals of GaP, InP, and, with suitable temperature profiles, $Ga_{1-x}In_xP$.

In addition to method modifications, significant progress has been made in reducing background contamination of the melt and improving crystalline perfection. Use of the more exotic refractory materials such as AlN and BN has reduced silicon contamination of the melt, especially in the LEC and Stockbarger methods. The silicon contamination from SiO_2 vessels, especially in the horizontal Bridgman method, has been reduced by a chemical trick. Silicon contamination in GaAs occurs because of the reaction of Ga with SiO_2 to produce Ga_2O vapor and Si. Even though SiO_2 is much more stable than the oxides of Ga and As, the reaction still produces silicon contamination and unwanted n-type doping of about 5×10^{16} to 50×10^{16} Si atoms per cubic centimeter of melt. This exceeds the desired controlled doping levels for several applications. The chemical trick to reduce silicon contamination is to add Ga_2O_3 to the Ga melt prior to synthesis. The Ga_2O_3 reacts

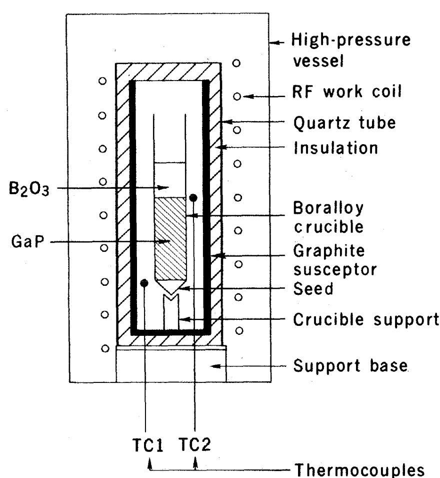

Fig. 5. Schematic of modified Stockbarger method for bulk crystal growth.

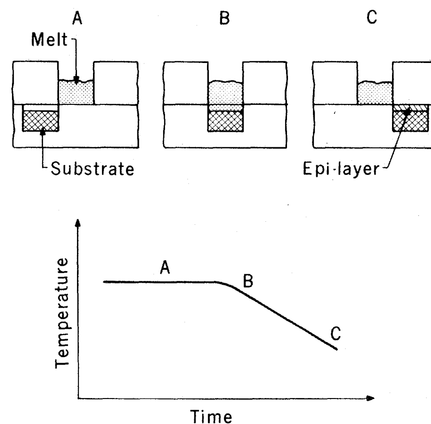

Fig. 6. Simplified representation of the liquid phase epitaxy method.

readily with Ga to produce Ga_2O vapor before the Ga reacts with the SiO_2 during heat-up. The initial presence of Ga_2O vapor greatly suppresses further reaction of the Ga with SiO_2, according to the mass action laws of chemistry. This technique has been used to form the highest-purity bulk GaAs reported to date. The semi-insulating form of this material contains $< 10^{15}$ electrically active impurities. Until recently, most semi-insulating GaAs was of lower purity and was made by overcompensating the n-type silicon contamination with Cr during growth. The Cr acts as an efficient donor compensating dopant in GaAs, but does not significantly dope the crystal p-type. Unfortunately, this type of semi-insulating GaAs produced some problems in the fabrication of GaAs MESFET structures, and therefore methods that produce high-purity semi-insulating GaAs are very desirable. Semi-insulating GaAs of intermediate purity was made recently by using BN vessels and the LEC method.

Improvements in the control of crystal perfection have been made on a somewhat limited scale. For example, the horizontal Bridgman method has been modified to allow the seeding of GaAs crystals on fixed orientations. It has been found that dislocation-free crystals can be grown with the [031] direction parallel to the crystal axis. So far, this has been limited to relatively small ingots about 200 grams in weight and 1.5 square centimeters in cross section. Dislocation-free GaAs has also been grown sporadically by the older modified Czochralski methods, but it has not yet been prepared by the LEC method.

To summarize the state of the art, GaAs crystals 5.0 to 7.0 cm in diameter and of moderate purity can be grown commercially by the LEC method. These crystals can be doped n-type

This content downloaded on Mon, 25 Feb 2013 12:12:51 PM
All use subject to JSTOR Terms and Conditions

($10^{16} < n < 5 \times 10^{18}$ cm^{-3}), *p*-type ($5 \times 10^{16} < p < 2 \times 10^{19}$ cm^{-3}), and semi-insulating (resistivity $>10^6$ ohm-cm). Currently, the most widely used semi-insulating material is doped with Cr. Commercial GaAs crystals of lower purity grown by the horizontal Bridgman method are also available with about the same doping ranges. The horizontal Bridgman material usually has a lower dislocation density and produces noncircular wafers. In the laboratory, it is possible to grow high-purity (ionized impurities $<10^{15}$ cm^{-3}), dislocation-free GaAs with a 1.5-cm^2 cross section.

Two other widely used III-V compounds, InP and GaP, are commercially available as bulk crystals and substrates. These are grown primarily by the LEC method. Except for AlP and AlAs, which are difficult to form into bulk crystals even by special techniques, the other materials in Table 2 with low dissociation pressures ($<10^{-3}$ atm) are usually available on special order and do not pose special problems for crystal growth in the research laboratory.

Thin-Film Fabrication

Most III-V device fabrication begins with deposition of one or more active epitaxial layers. Epitaxial layers are those which conform to the crystal structure and orientation of the material on which they are deposited. There are three principal epitaxial techniques for III-V materials: liquid phase epitaxy (LPE), chemical vapor deposition (CVD), and molecular beam epitaxy (MBE). The MBE method is discussed in another article in this issue (*5*).

The LPE method has been the most widely used one for thin-film III-V materials and device research. It was first developed in the late 1950's and applied to the formation of *p-n* junctions in germanium and GaAs. In the LPE method a solid solute phase is epitaxially grown by supercooling a melt or solvent containing the solute. For III-V materials, this generally means that the melt composition is rich with respect to one of the group III element in the solid phase. For example, LPE growth of $Ga_{1-x}Al_xAs$ is generally performed by using a melt of more than 90 percent Ga, the rest being Al, As, and some dopant. The term LPE originally referred to supercooling melts—lowering the temperature of melts that were in solid-liquid equilibrium. More recently the technique has been expanded to include growth from melts that are supersaturated by methods other than supercooling. Over the years many LPE apparatuses and procedures have been developed, and they cannot be adequately discussed here. It is more useful to examine the nature of the LPE method in terms of its wide use as a research tool and to a lesser extent its use in production lines, and also to discuss some recent innovations that attempt to overcome some disadvantages of the method.

The "typical" LPE method is shown schematically in Fig. 6. The basic features are a melt chamber of fixed geometry and a method for moving a substrate in and out of the melt. Usually, operation begins by establishing a melt at solid-liquid equilibrium with the substrate removed from the melt region. The melt is usually supercooled by lowering the temperature at a constant rate. The substrate is then brought into contact with the melt while maintaining the cooling. After a prescribed change in temperature or elapsed time, the substrate is removed from the melt. For small cooling rates and small melt volumes, nearly equilibrium growth occurs since the composition of the melt remains near the liquidus line of the phase diagram. The composition and layer thickness are then mainly a function of the temperature change during substrate-melt contact. For large cooling rates and large melt volumes, the composition of the melt at the solid-liquid interface is very close to the liquidus composition, while the bulk of the melt is of a different composition. This results in diffusion-controlled growth, and hence for small temperature changes the layer thickness and composition are mainly a function of time of substrate-melt contact.

Table 3 shows notable advantages and disadvantages of the LPE method. Perhaps the most important advantage of the technique, especially in the exploratory research environment, is the beneficial role of the solid-liquid interface in terms of quality of grown material. This is because melts of group III elements can be made with high purity. Also, as growth of the solid layer proceeds from LPE melts, most impurities in the melt

Table 2. Some physical and thermochemical properties of III-V compounds relevant to bulk crystal growth.

Compound	Lattice constant (Å)	Band gap (eV) and type (D, I)*	Dissociation pressure (atm)	Melting point (°C)
AlP	5.45	2.45 I	8	1840
GaP	5.45	2.24 I	35	1465
AlAs	5.66	2.16 I	1.4	1760
AlSb	6.14	1.5 I	$< 10^{-3}$	1065
GaAs	5.65	1.4 D	1	1240
InP	5.87	1.35 D	25	1065
GaSb	6.10	0.72 D	$< 10^{-3}$	706
InAs	6.06	0.35 D	0.3	947
InSb	6.48	0.18 D	$< 10^{-3}$	525

*Direct or indirect.

Table 3. Comparison of the LPE and CVD methods.

LPE	CVD
Advantages	
Near-equilibrium growth conditions	In situ substrate cleaning or etching
Growth of material with good optical and electrical properties	Good morphology and thickness control
Liquid-solid interface lowers contamination of layer during growth	Good doping control
High-purity melts	Low-temperature growth (600° to 800°C)
Nonreactive melt containers	Multilayer and multijunctions easily grown
Low-temperature growth (600° to 800°C)	Growth start and termination well defined
Low defect densities	Large-scale production
Melt getters impurities from solid layer	In situ process monitoring; for example, ellipsometry and IR spectrometry
Disadvantages	
Imprecise thickness and morphology control due to variable growth mechanism, terracing, and meniscus line effects	Ultrapure chemicals required
Growth termination a fundamental problem	Leak-free systems required for high-purity materials with good optical properties
Unfavorable phase diagrams for growth of some III-V alloys	Vapor phase reactants may produce defects, traps, or unwanted doping in epilayer
Cross-doping effects of volatile dopants in multimelt systems	Reactivity of chemicals with containment vessels
Large batch or continuous processing of multilayer structures very difficult	Autodoping of epilayer by substrate etching during growth

This content downloaded on Mon, 25 Feb 2013 12:12:51 PM
All use subject to JSTOR Terms and Conditions

tend to be rejected rather than incorporated into the layer. These effects together mean that useful materials can be grown by "quick and dirty" experiments. An example of this was the LPE growth of $Ga_{1-x}Al_xAs$ layers. High-efficiency $Ga_{1-x}Al_xAs$ LED devices were first made around 1967 by this method. It has taken more than 10 years of intensive research to duplicate the quality of this material by the CVD and MBE methods.

There are two principal disadvantages of this method applied to III-V materials. To terminate growth by the LPE method, the melt must be physically separated from the substrate at the end of the growth period. Failure to do this would result in unwanted growth during the return of the apparatus to room temperature, because the solubility of the solute species decreases with decreasing temperature. In the early development of LPE methods, much effort was devoted to designing apparatus with features that would cleanly shear away the melt from the substrate. In addition, much effort was spent on multichamber fixtures to contain several different melts in order to grow multiple *p-n* and heterojunction structures. Consequently, most of the currently interesting optoelectronic heterostructure devices were pioneered by the LPE method, and the method is still the preferred technique for many of these devices.

Another disadvantage of the LPE method is the rough surface morphology associated with the near-equilibrium growth kinetics and melt separation dynamics. Terrace-like surfaces and interfaces occur as a result of a slight misorientation of the substrate surface with respect to a low-index crystallographic plane. Meniscus line motion during melt separation produces trails on surfaces and interfaces. Recently, several advances have been made in the LPE method to improve surface morphology. Studies of melt supersaturation and substrate orientation have led to an understanding of the conditions necessary for LPE growth of smooth surfaces and planar layers and interfaces. It has been found that smooth surfaces can be grown under conditions of large melt supersaturations and critical substrate orientation. Specialized techniques have been developed for achieving controlled melt supersaturation. They include electroepitaxy, in which electric current flowing across the solid-liquid interface causes localized cooling and melt supersaturation, and isothermal melt mixing techniques, in which equilibrium melts of different compositions are mixed at constant temperature to produce a supersaturated melt. The principles of critically oriented substrates for achieving microscopically smooth epitaxial layers are based on the interplay of the variation of interface free energy with crystallographic direction, the interface area, and the interface configuration that minimizes its total energy during growth.

A device-material-method menu illustrating the use of the LPE method is shown in Table 4. Much of the LPE research is focused on the following devices and materials: MESFET's of GaAs, InP, and $In_{1-x}Ga_xAs$; injection lasers of GaAs-$Ga_{1-x}Al_xAs$ and InP-$Ga_{1-x}In_xAs_{1-y}P_y$; photodetectors and solar cells of InAs, InSb, $Ga_{1-x}In_xSb$, and GaAs-$Ga_{1-x}Al_xAs$; and LED's of GaP, GaAs, and $Ga_{1-x}Al_xAs$. I believe that as the demand for greater device dimension control increases, the role of the LPE method in the laboratory will diminish in favor of the CVD and MBE methods. There is evidence that this trend has already started, and that ulti-

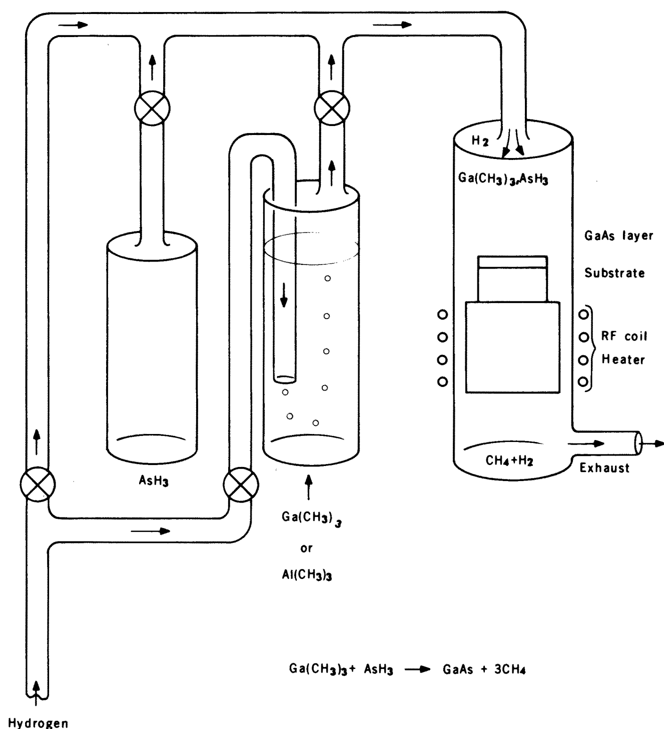

Fig. 7. Simplified diagram of the metal-organic method for chemical vapor deposition.

Table 4. Exemplary III-V materials and devices and epitaxial methods used for fabrication.

Device	Material	Method
LED	GaAs:Si-doped	LPE
	$Ga_{1-x}Al_xAs$-GaAs	LPE, CVD
	$GaAs_{1-x}P_x$	CVD
	$Ga_{1-x}In_xAs_{1-y}P_y$-InP	LPE, CVD
	GaP	LPE, CVD
DH laser	GaAs-$Ga_{1-x}Al_xAs$	LPE, CVD
	InP-$Ga_{1-x}In_xAs_{1-y}P_y$	LPE, CVD
Solar cell	GaAs-$Ga_{1-x}Al_xAs$	LPE, CVD
	n-p-GaAs	CVD
	InP-CdS	CVD
IR photodetector	InSb	Bulk
	$Ga_{1-x}In_xAs_{1-y}P_y$	LPE, CVD
	$GaAs_{1-x}Sb_x$	LPE, CVD
	InAs	Bulk
Heterojunction transistor	GaAs-$Ga_{1-x}Al_xAs$	LPE, CVD
	InP-$Ga_{1-x}In_xAs_{1-y}P_y$	LPE, CVD
Negative electron affinity device	GaAs	LPE, CVD
	GaP	LPE, CVD
	$Ga_{1-x}In_xAs_{1-y}P_y$	LPE, CVD
MESFET	GaAs	LPE, CVD
	InP	LPE, CVD

This content downloaded on Mon, 25 Feb 2013 12:12:51 PM
All use subject to JSTOR Terms and Conditions

mately the LPE method will be used for specialized applications in which it offers some advantage for materials quality or device structure.

The CVD method is sometimes referred to as vapor phase epitaxy (VPE) to distinguish it from the more generalized chemical vapor deposition method used to form both epitaxial and nonepitaxial films by thermochemical vapor phase reactions. Most of the research on CVD applied to III-V materials has concentrated on two different chemistries: (i) the III-halogens and V-halogens or V-hydrogen, such as $GaCl_3$ and $AsCl_3$ or AsH_3, and (ii) the III metal-organics and V-hydrogen, such as $Ga_3(CH_3)$ and AsH_3. The thermochemistries of these systems are very different. The halogen reactions are usually "hot" to "cold" ones, in which the III-halogen is generated in a hot zone by reaction of the III element with HCl and then diffuses to the cold zone, where it reacts with the V species to form the III-V material. The metal-organic (MO) chemistry is a "hot wall" process in which the III-R compound "cracks" or pyrolyzes away the organic (R) group and the remaining III and VH_3 react to form III-V. A schematic of the MO methods applied to GaAs is shown in Fig. 7.

Both of these chemistries have been widely developed and used successfully for GaAs devices. For other III-V compound and alloys, the situation is somewhat confusing and is changing rapidly. The halogen techniques were more intensely studied than the MO method early in the development of III-V materials. During this period several important devices were developed with the halogen method, most notably the $GaAs_{1-x}P_x$ LED and the GaAs Gunn effect device. Others include $In_{1-x}Ga_xP$ LED's and lasers. Until very recently, the MO technique was not developed to the point of fabricating some of the important devices. When success did occur, it was on GaAs-$Ga_{1-x}Al_xAs$-based devices, which at the time were practically inaccessible by the halogen method, primarily because of unfavorable thermochemistry and reactivity of containing vessels. Since the success of the MO method with $Ga_{1-x}Al_xAs$, there have been increased efforts to extend it to other III-V materials. Many workers consider this method to have long-term advantages including better thickness, purity, and composition control and the ability to grow a wide range of III-V compounds and alloys.

Referring again to Table 3, it is useful to consider some of the advantages and disadvantages of the CVD method. The principal advantages are (i) good dimension control, (ii) good doping and composition control, and (iii) straightforward scale-up for wafer processing in a production environment. The principal disadvantages are (i) the requirement for ultrapure chemicals, (ii) high reactivity of the vapor with containment vessels, and (iii) possible introduction of defects or unwanted doping by chemical reactants from the formation of the III-V material. A reexamination of Table 4 shows that the CVD method has been successfully applied to the most currently important devices.

Conclusions

At present, silicon-based devices dominate the semiconductor device industry. The impact of III-V materials so far has been on specialty optoelectronic devices, including lasers, LED's, photodetectors, and solar cells. This has been due mainly to the large variety of band-gap energies available with alloying of III-V compounds, the formation of lattice-matched heterojunctions, special impurities that enhance radiative recombination, bulk crystal growth techniques that produce useful substrates, and the development of the LPE and CVD methods for producing dimensionally controlled epitaxial layers of good optical and electrical quality. As integrated circuits become more dense and complicated, research in this field must consider material, device, and processing as a unit. The future role of III-V materials is likely to be significant because of their processing advantages associated with the chemical and functional aspects of structures similar to those found in optoelectronic devices.

References and Notes

1. The III and V refer to the group IIIA and group VA elements of the periodic table, respectively.
2. It is even more appropriate that material, device, processing, and packaging be considered as a unit for high-speed data-processing applications.
3. It was not the first choice of the pioneers of the transistor industry. Shockley and Bardeen worked unsuccessfully for a decade on CuO, which was attractive for integration with copper wires. They finally succeeded in showing bipolar transistor action after switching to germanium. It was only after the U.S. government's insistence on high-temperature operation for military purposes forced the development of silicon that the great advantages of that material and its uniquely high-quality passivating oxide were discovered.
4. For a more complete description, the interested reader is encouraged to consult C. J. Nuese, *J. Electron Mater.* **6**, 253 (1977); A. A. Bergh and P. J. Dean, *Proc. IEEE* **60**, 156 (1972); C. B. Duke and N. Holonyak, Jr., *Phys. Today* (Dec. 1973), p. 23; M. G. Craford and W. O. Groves, *Proc. IEEE* **61**, 862 (1973); S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1969); A. G. Milnes and D. L. Feucht, *Heterojunctions and Metal-Semiconductor Junctions* (Academic Press, New York, 1972); H. Hovel, *Solar Cells*, vol. 11, *Semiconductors and Semimetals* (Academic Press, New York, 1975); J. W. Matthews, *Materials Science and Technology—Epitaxial Growth* (Academic Press, New York, 1975); P. Hartman, *Crystal Growth: An Introduction* (North-Holland, Amsterdam, 1973); G. M. Blom, Ed., *J. Cryst. Growth* **27** (1974); H. Nelson, *RCA Rev.* **24**, 603 (1963); J. M. Woodall, *J. Electrochem. Soc.* **118**, 150 (1971); H. Rupprecht, J. M. Woodall, G. D. Pettit, *Appl. Phys. Lett.* **11**, 81 (1967); J. M. Woodall, *Trans. Metall. Soc. AIME* **239**, 378 (1967); S. E. Blum and R. J. Chicotka, *J. Electrochem. Soc.* **120**, 588 (1973); M. B. Small, K. H. Bachem, R. M. Potemski, *J. Cryst. Growth* **39**, 216 (1977); J. C. C. Fan, C. O. Bozler, B. J. Palm, *Appl. Phys. Lett.* **35**, 875 (1979); Y. Imamura, L. Jastrzebski, H. C. Gatos, *J. Electrochem. Soc.* **126**, 1381 (1979); M. G. Craford and N. Holonyak, Jr., in *Optical Properties of Solids*, B. O. Seraphin, Ed. (Gordon & Breach, New York, 1976), p. 188; D. J. Wolford, B. G. Streetman, R. J. Nelson, N. Holonyak, Jr., *Solid State Commun.* **19**, 741 (1976); D. J. Wolford, B. G. Streetman, W. Y. Hsu, J. D. Dow, R. J. Nelson, H. Holonyak, Jr., *Phys. Rev. Lett.* **36**, 1400 (1976).
5. M. Panish, *Science* **208**, 916 (1980).

This content downloaded on Mon, 25 Feb 2013 12:12:51 PM
All use subject to JSTOR Terms and Conditions